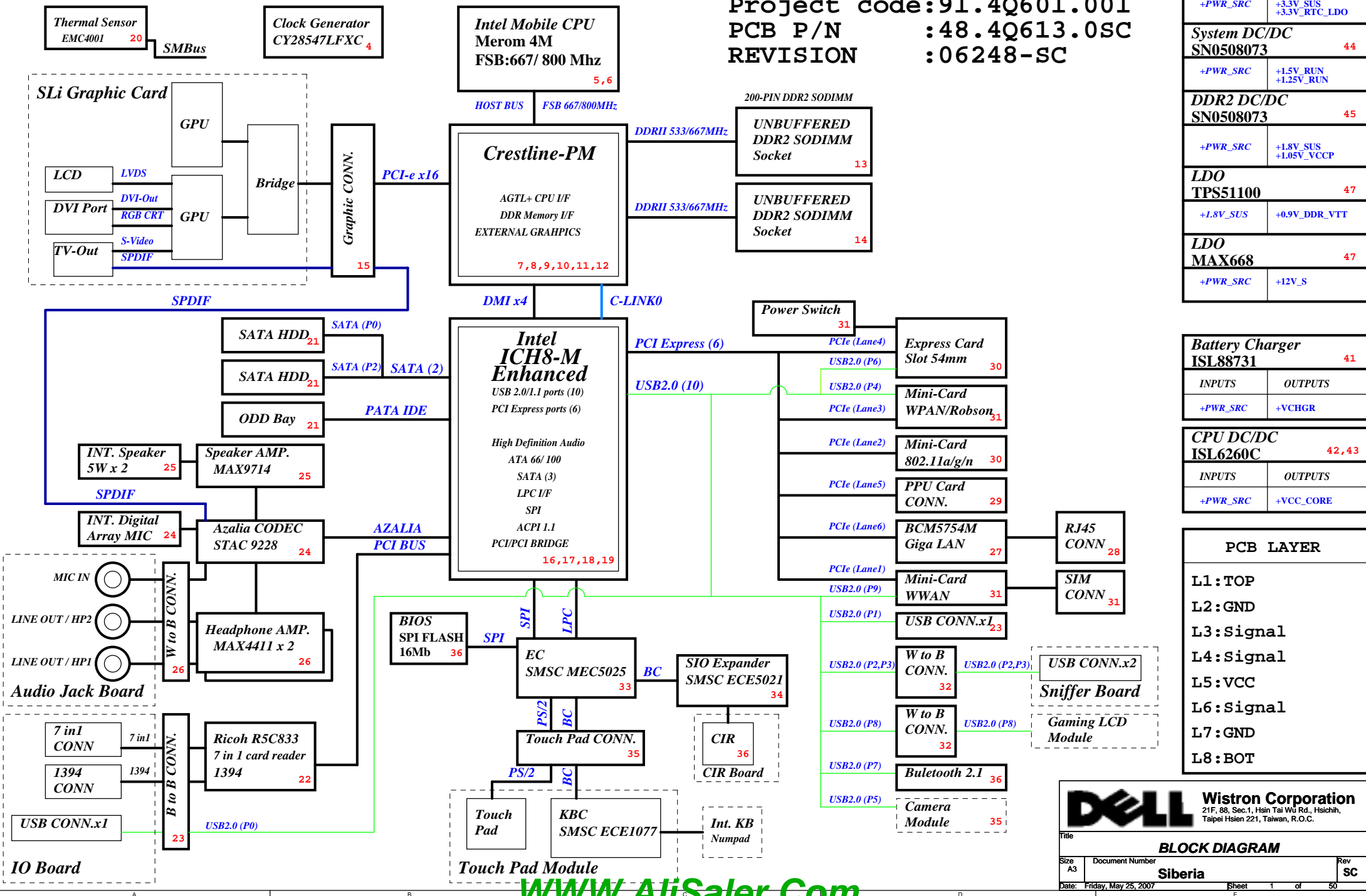


# Siberia Block Diagram

Project code: 91.4Q601.001  
PCB P/N : 48.4Q613.0SC  
REVISION : 06248-SC



# WWW.AliSaler.Com

## CLOCK GEN CY28547

### 27M\_SS/LCD96\_100M SELECTION TABLE

#### BYTE 10

Bit5 S1	Bit4 S0	Spread Spectrum S[1:0]
0	0	-0.5%(Default)
0	1	-1.0%
1	0	-1.5%
1	1	-2.0%

#### BYTE 15

##### IO\_VOUT[2,1,0]

Bit2 IO_VOUT2	Bit1 IO_VOUT1	Bit0 IO_VOUT0	IO_VOUT[2,1,0]
0	0	1	0.3V
0	0	1	0.4V
0	1	0	0.5V
0	1	1	0.6V
1	0	0	0.7V
1	0	1	0.8V(Default)
1	1	0	0.9V
1	1	1	1.0V

SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB
1	0	1	100M	X
0	0	1	133M	X
0	1	1	166M	667M
0	1	0	200M	800M

## INTEL CRESTLINE STRAP PIN

CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 19 DMI Lane Reserved	Normal Operation	Lane Reserved
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous
SDVO_CTRL_DATA	NO SDVO Card Present	SDVO Card Present

CFG 12	XOR/ALL-Z
CFG 13	Reserved
LL(00)	XOR Mode Enabled
HL(01)	All Z Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation

## PCIE Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	BT/UWB/Robson
LANE4	Express Card
LANE5	PPU card
LANE6	Giba Bit LOM

## PCI ROUTING

	IDSEL	INT	REQ	GNT
1394/MediaCard	AD17	C D	1	1

## USB TABLE

#### ICH

USB0	Ext Lift Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

## INTEL ICH8-M STRAP PIN

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config 1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low at rising edge of PWROK.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers:offset 224h)
HDA_SYNC	PCIE Port Config 1 bit0, Rising Edge of PWROK.	Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE Port Config 2 bit0, Rising Edge of PWROK.	Sets bit2 of RPC.PC(Config Registers:Offset 224h)
GPIO20	Reserved. Rising Edge of PWROK.	Weak Internal PULL-DOWN.NOTE:This signal should not be pull HIGH.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0# SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05 VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05,VccSus1_5 and VccCL1_5 VRM when sampled high
LAN100_SLP	Integrated VccLAN1_05 VccCL1_05 VRM enable /Disable. Always sampled.	Enables integrated VccLAN1_05,VccCL1_05 VRM when sampled high
SATALED#	PCIE LAN REVERSAL.Rising Edge of PWROK.	This signal has weak internal pull-up. set bit27 of MPC.LR(Device28:Function0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8M will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.(Offset:3410h:bit5)
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK_EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK.	Internal Pull-Up.If sampled low,the Flash Descriptor Security will be overridden.if high,the Security measures defined in the Flash Descriptor will be in effect. This should only be used in manufacturing environments

XOR Chain Entrance Strap		
ICH_RSVP3	AZ_DOUT ICH	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation(Default)
1	1	Set PCIE port cofig bit1

A16 swap override strap		
PCI_GNT#3	low = A16 swap override enable	high = default
BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPI
1	0	PCI
1	1	LPC(Default)

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
SM_INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

DEFAULE HIGH

No Reboot Strap	
SPKR	LOW = Default
	High=No Reboot

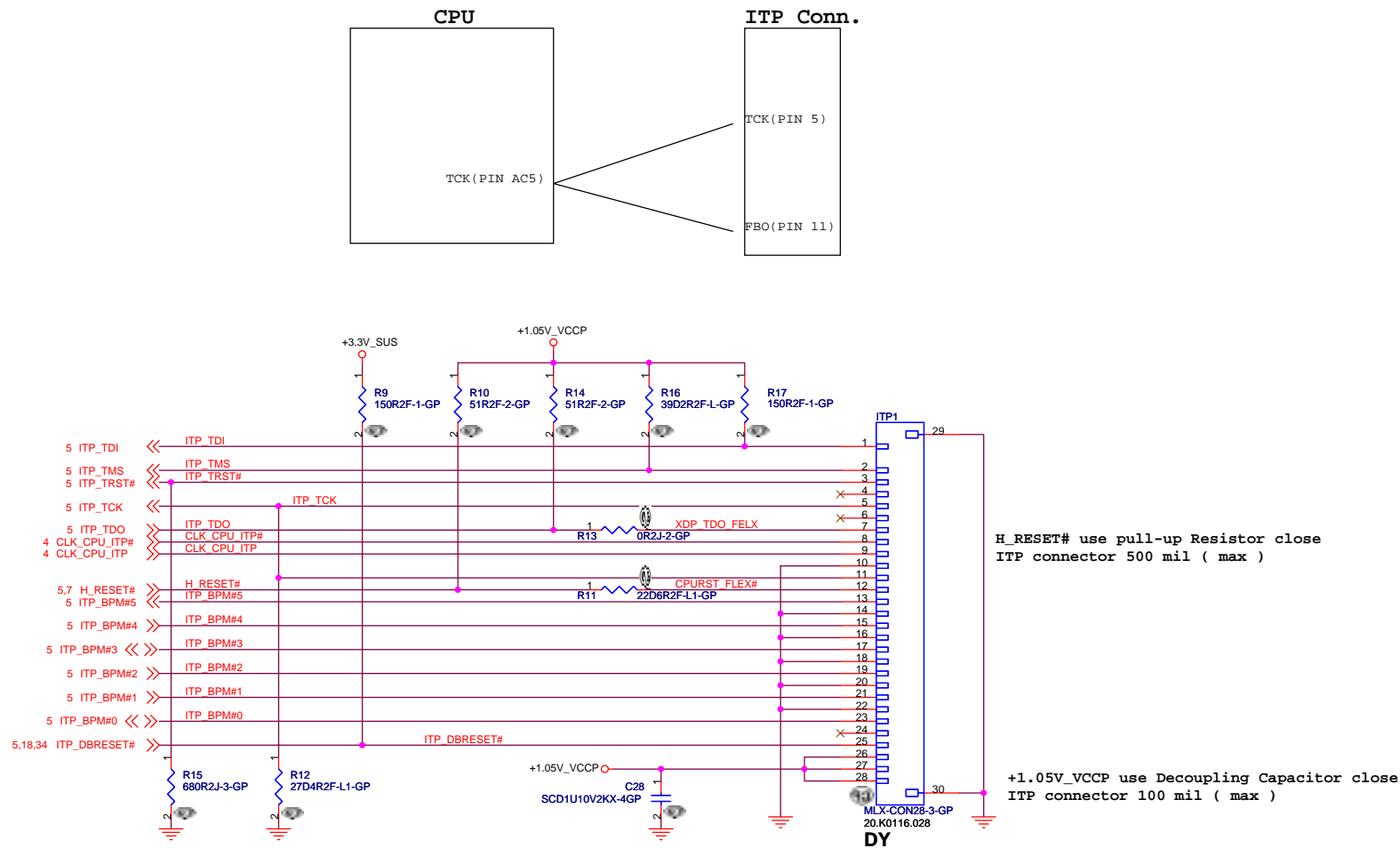
8.2K PULL HIGH

## INTEL ICH8-M INTEGRATED PULL-UPS and PULL-DOWNS

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FWH[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST0#	PULL-UP 13K



Table of Content		
Size A3	Document Number	Rev SC
Date: Friday, May 25, 2007	Siberia	Sheet 2 of 50



**ITP Debug Conn.**

<Variant Name>



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Title

**ITP Debug**

Size  
A3

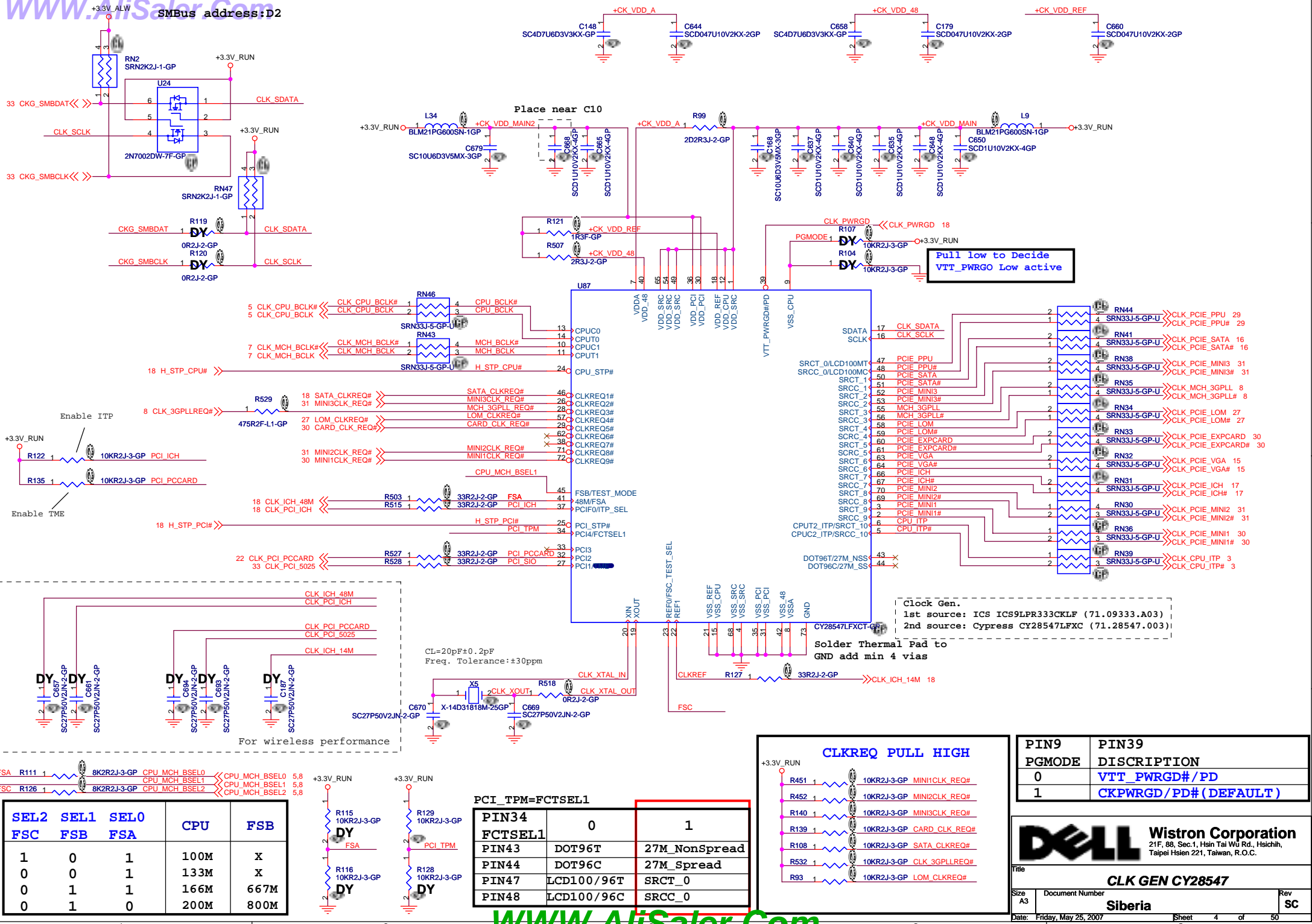
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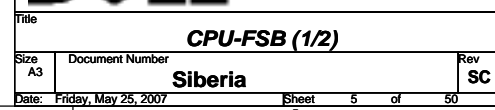
**Siberia**

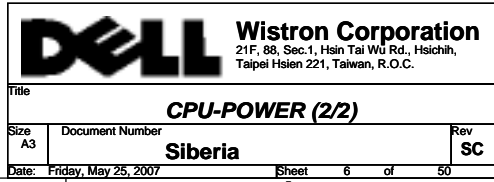
Rev  
SC

Date: Friday, May 25, 2007

Sheet 3 of 50





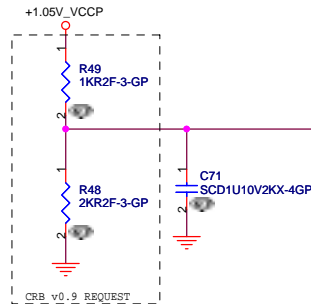




H\_D#[63..0] <<>> H\_D#[63..0] 5  
H\_A#[35..3] <<>> H\_A#[35..3] 5  
H\_REQ#[4..0] <<>> H\_REQ#[4..0] 5  
H\_RS#[2..0] >>> H\_RS#[2..0] 5



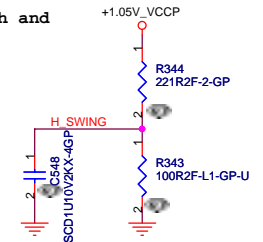
H\_REF Decoupling Crestline  
close Crestline 100 mil



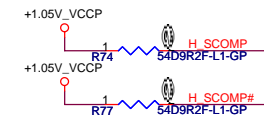
H\_SWING routing Trace width and  
Spacing use 10 / 20 mil

H\_SWING Resistors and  
Capacitors close  
Caliistoga 500 mil ( MAX )

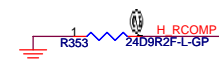
From Schematic Design  
Checklit v.1201  
221 1% pull high 100  
1% pull low



H\_SCOMP and H\_SCOMP# Resistors  
and Capacitors close Caliistoga  
500 mil ( MAX )  
Zo=55ohms

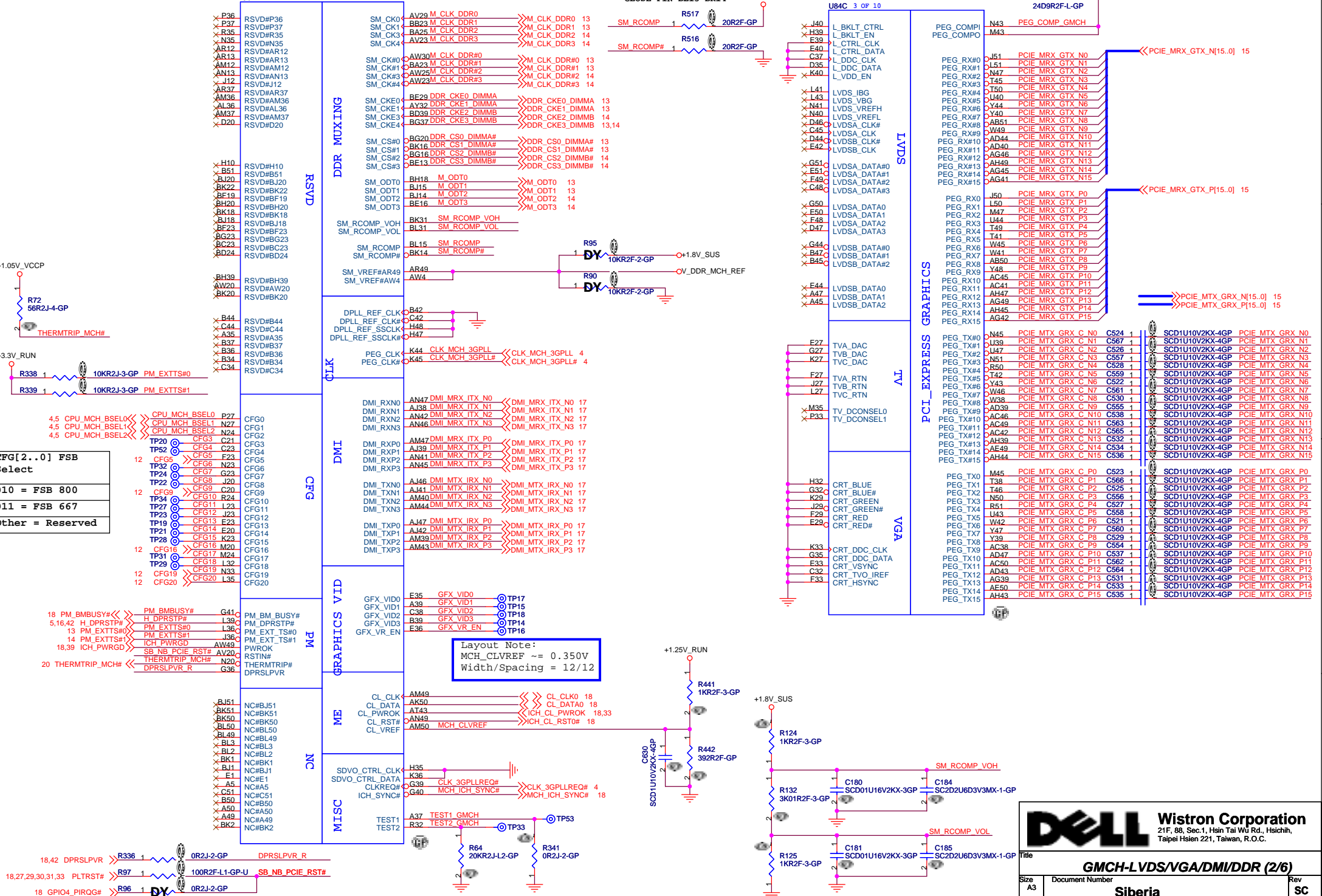


H\_RCOMP routing Trace width and  
Spacing use 10 / 20 mil

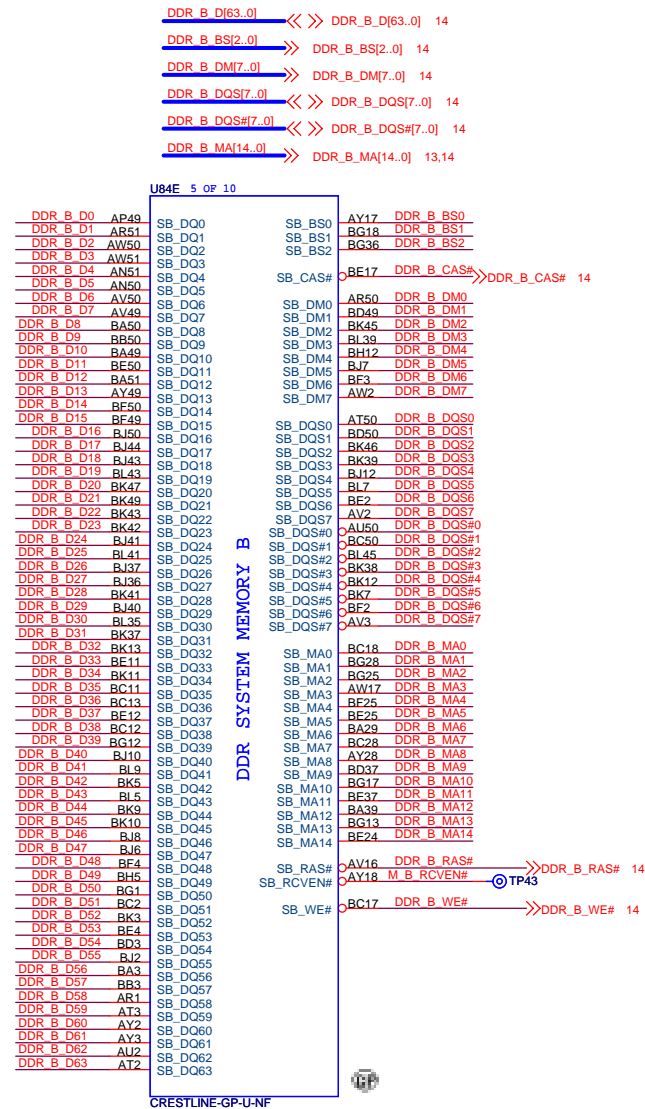
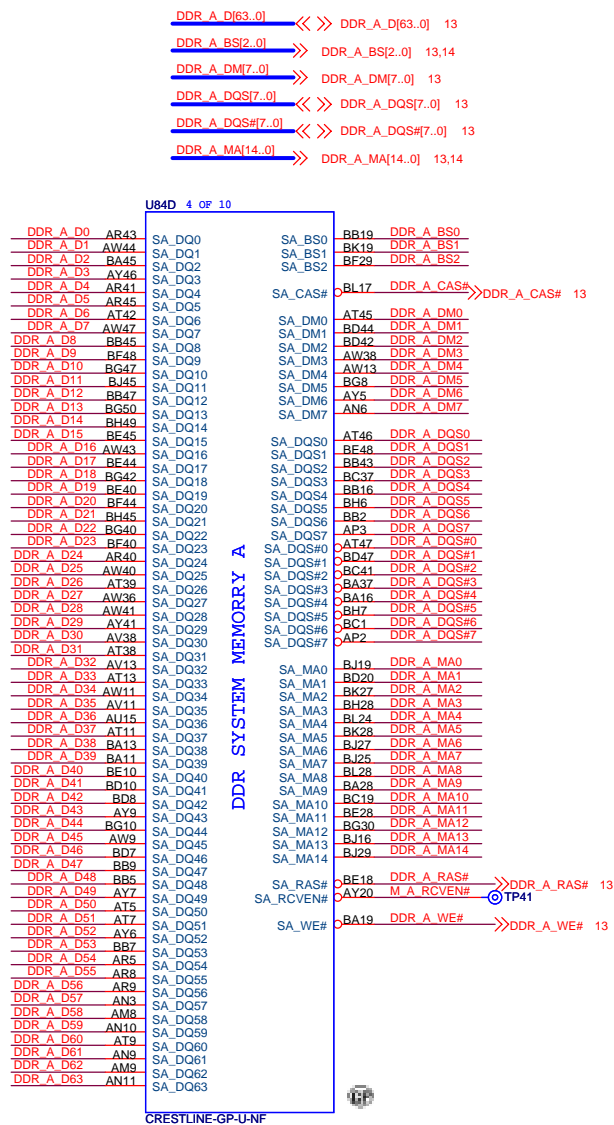


**DELL** Wistron Corporation  
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Title  
**GMCH-FSB LIBC (1/6)**  
Size A3 Document Number  
**Siberia**  
Date: Friday, May 25, 2007 Sheet 7 of 50  
Rev SC

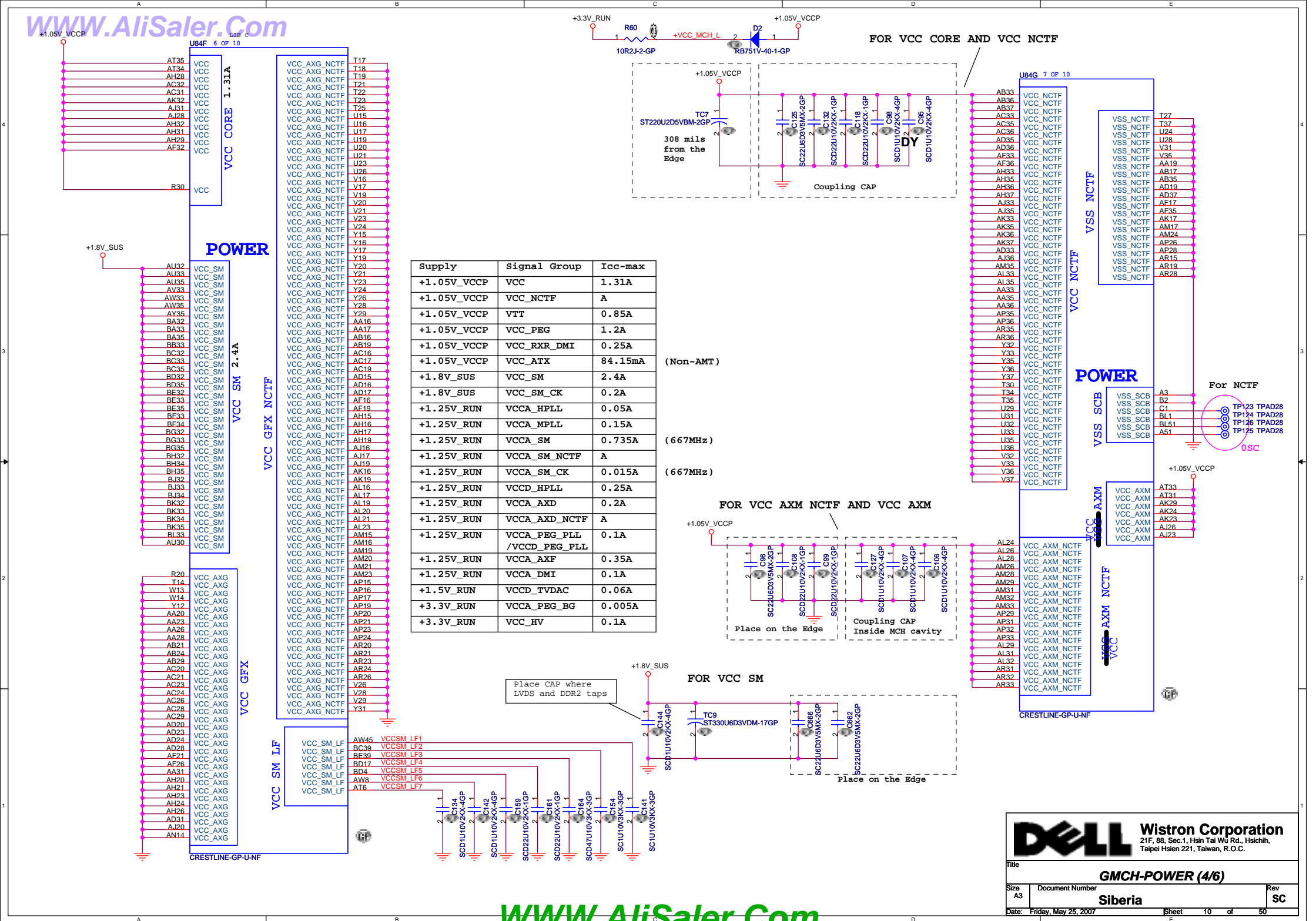






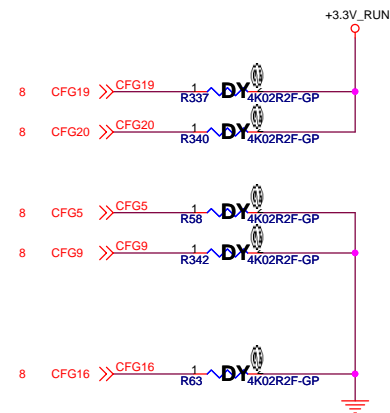
**Wistron Corporation**  
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Taipei Hsien 221, Taiwan, R.O.C.

Title			GMCH-DDR (3/6)	
Size	Document Number	Siberia		Rev
A3				SC
Date:	Friday, May 25, 2007	Sheet	9	of 50



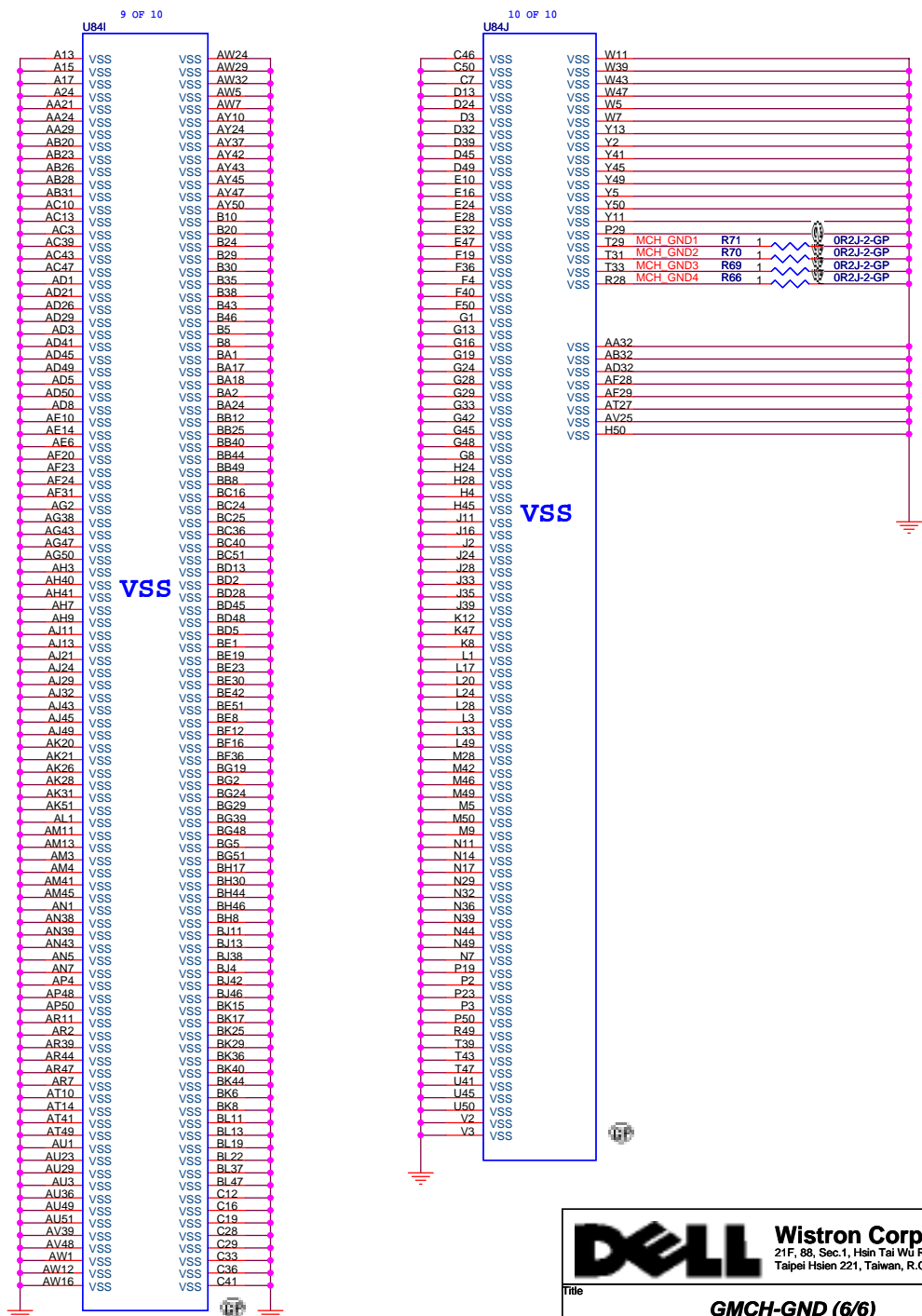


**Layout Note:**  
Location of all MCH CFG strap resistors need to be close to trace to minimize stub



CFG Strap	LOW 0	HIGH 1
CFG 5	DMI X 2	DMI X 4
CFG 9 PCI Express Graphics Lane Reversal	Lane Reversal	Normal Mode(Lanes number in order)
CFG 16 FSB Dynamic ODT	Disabled	Enabled
CFG 18 VCC select	1.05V	1.5V
CFG 19 DMI Lane Reserved	Normal Operation	Reserved Lane
CFG 20 Concurrent SDVO/PCIE	Only PCIE or SDVO is operation	PCIE and SDVO are operation simultaneous

CFG 12 CFG 13	XOR/ALL-Z
LL(00)	Reserved
LH(01)	XOR Mode Enabled
HL(10)	All Z Mode Enabled
HH(11)	Normal Operation



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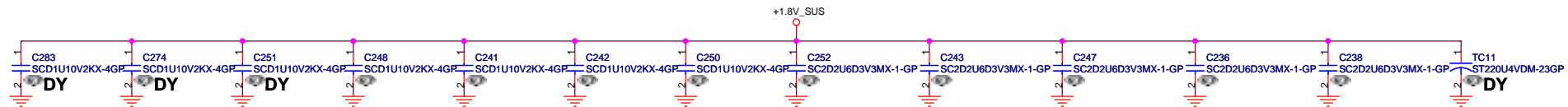
Title: **GMCH-GND (6/6)**

Size A3 Document Number **Siberia** Rev **SC**

Date: Friday, May 25, 2007 Sheet 12 of 50

<u>DDR_A_DM[7..0]</u>	◀	DDR_A_DM[7..0]	9
<u>DDR_A_DQS[7..0]</u>	◀	DDR_A_DQS[7..0]	9
<u>DDR_A_DQS#[7..0]</u>	◀	DDR_A_DQS#[7..0]	9
<u>DDR_A_D[63..0]</u>	◀	DDR_A_D[63..0]	9
<u>DDR_A_BS[2..0]</u>	◀	DDR_A_BS[2..0]	9,14
<u>DDR_A_MA[14..0]</u>	◀	DDR_A_MA[14..0]	9,14

(Reverse Type)  
DIMM 1(BOT side)  
DIMM 2(BOT side)



+0.9V\_DDR\_VTT

C690 SCD1U10V2KX-4GP C215 SCD1U10V2KX-4GP C213 SCD1U10V2KX-4GP C216 SCD1U10V2KX-4GP C217 SCD1U10V2KX-4GP C214 SCD1U10V2KX-4GP

Pleace use One Capacitor close to every Two pull-up Resistors

C297 SCD1U10V2KX-4GP C688 SCD1U10V2KX-4GP C698 SCD1U10V2KX-4GP C689 SCD1U10V2KX-4GP C686 SCD1U10V2KX-4GP C699 SCD1U10V2KX-4GP C687 SCD1U10V2KX-4GP

**SWAP**

+0.9V\_DDR\_VTT

DDR\_A MA14 1 R161 4  
56R2J-4-GP

DDR\_A MA6 1 RN6 4  
DDR\_A MA2 2 3

SRN56J-4-GP RN7 4  
DDR\_A MA0 1 3  
DDR\_A RAS# 2 2

SRN56J-4-GP RN53 4  
DDR\_A MA5 1 3  
DDR\_A MA8 2 2

SRN56J-4-GP RN49 4  
M\_ODT1 1 3  
DDR\_CS1\_DIMMA# 2 2

SRN56J-4-GP RN9 4  
M\_ODT0 1 3  
DDR\_A MA13 2 2

SRN56J-4-GP RN54 4  
DDR\_A MA9 1 3  
DDR\_A MA12 2 2

SRN56J-4-GP RN5 4

DDR\_B MA11 1 RN52 4  
DDR\_CKE3\_DIMMB 2 3

DDR\_A CAS# 1 RN5 4  
DDR\_A WE# 2 3

SRN56J-4-GP RN8 4  
DDR\_A BS1 1 3  
DDR\_CS0\_DIMMA# 2 2

SRN56J-4-GP RN16 4  
DDR\_B MA11 1 3  
DDR\_CKE3\_DIMMB 2 2

SRN56J-4-GP RN50 4  
DDR\_A CAS# 1 3  
DDR\_A WE# 2 2

SRN56J-4-GP RN55 4  
DDR\_A BS2 1 3  
DDR\_CKE0\_DIMMA 2 2

SRN56J-4-GP RN4 4  
DDR\_CKE1\_DIMMA 1 3  
DDR\_A MA11 2 2

SRN56J-4-GP RN3 4

+0.9V\_DDR\_VTT

DDR_CS0_DIMMA#	DDR_CS0_DIMMA#	8
DDR_CS1_DIMMA#	DDR_CS1_DIMMA#	8
DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	8
DDR_CKE1_DIMMA	DDR_CKE1_DIMMA	8
DDR_A_RAS#	DDR_A_RAS#	9
DDR_A_CAS#	DDR_A_CAS#	9
DDR_A_WE#	DDR_A_WE#	9
M_ODT0	M_ODT0	8
M_ODT1	M_ODT1	8

**<Variant Name>**



Title

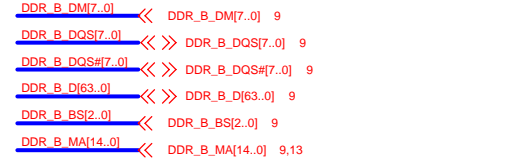
**DDR2-SODIMM1**

Size	Document Number	Rev
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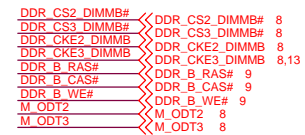
A3	<b>Siberia</b>	SC
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Date: Friday, May 25, 2007 Sheet 13 of 50





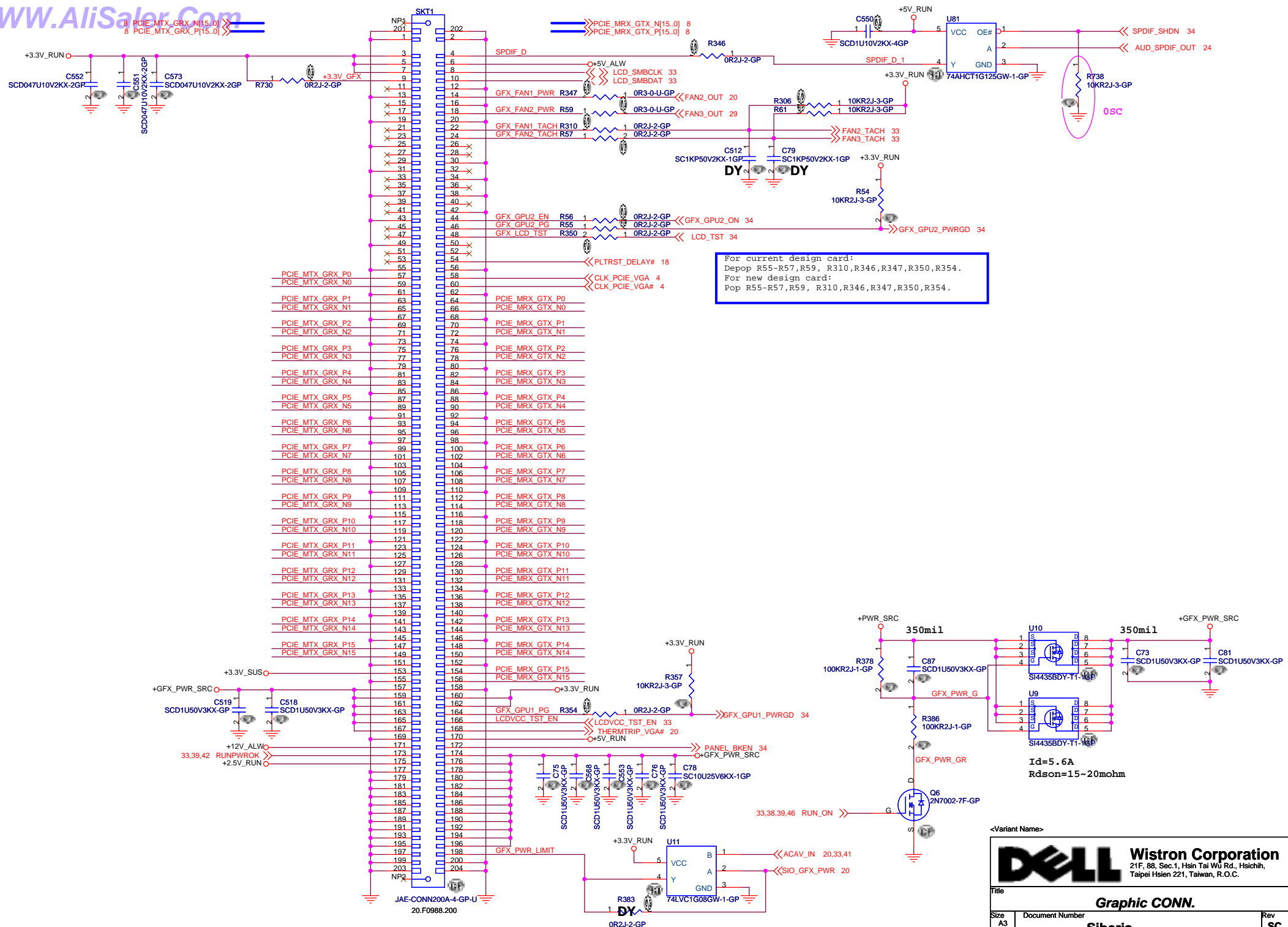
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62.10017.D41

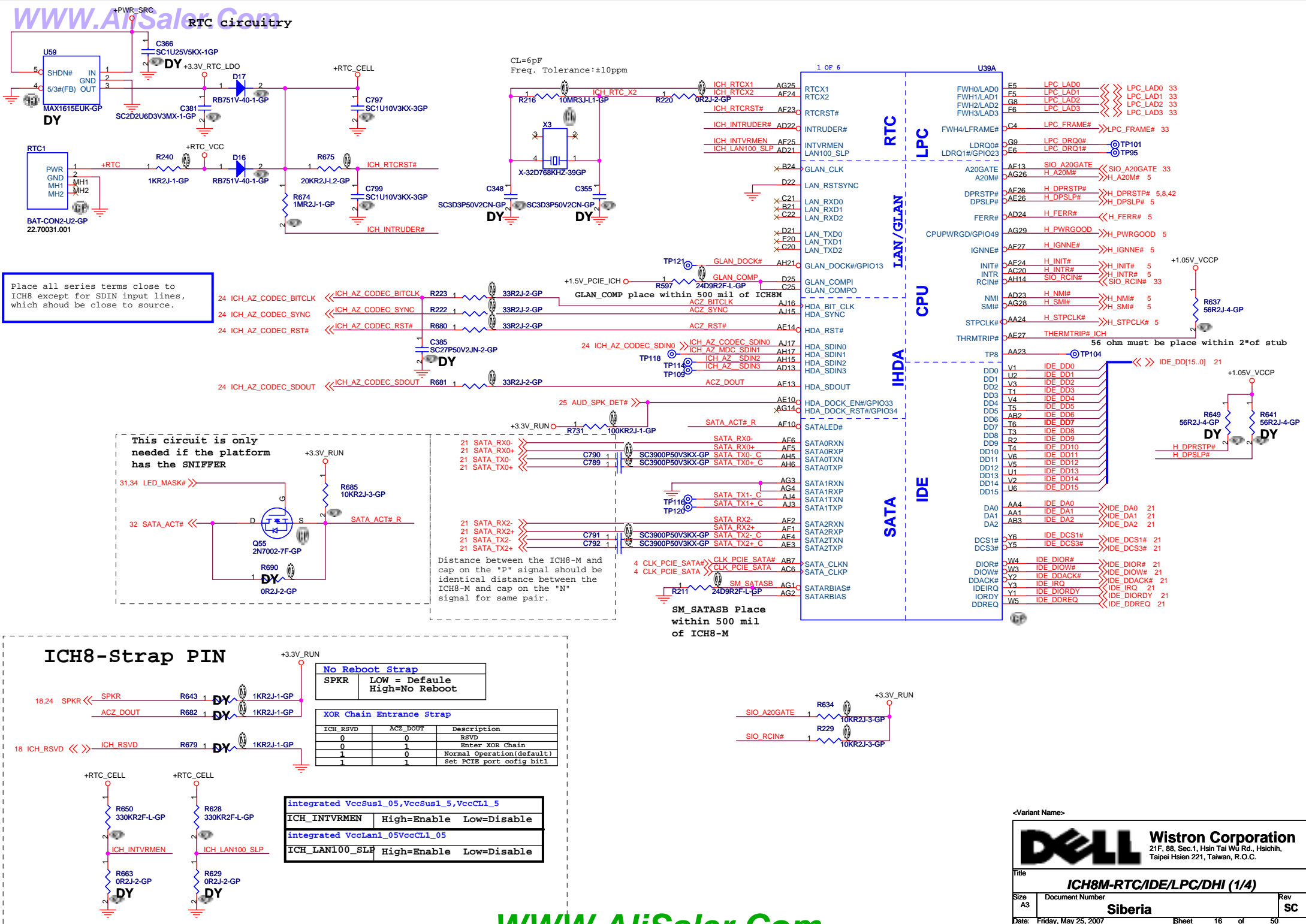


Others pull-up Resistors close  
DIMM Slot 750 mil ( MAX )



Rev	00
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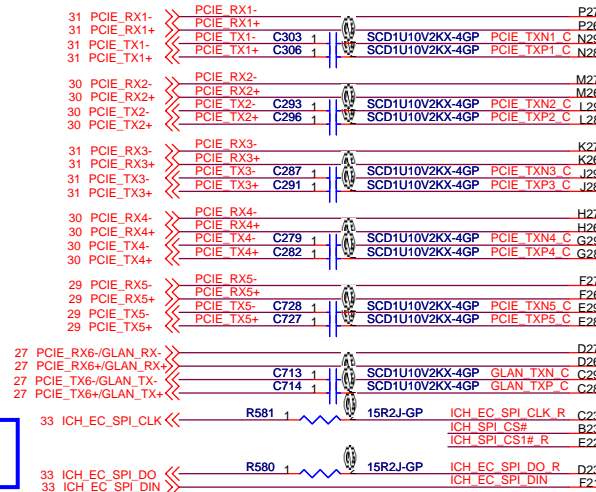




### PCIe Interface Routing

LANE1	MiniCard WWAN
LANE2	MiniCard WLAN
LANE3	MiniCard WPAN
LANE4	Express Card
LANE5	PPU Card
LANE6	Giba Bit LOM

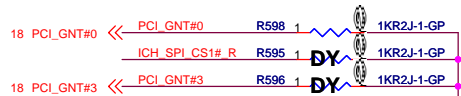
### PCIe TX dc blocking Capacitors close to ICH8-M



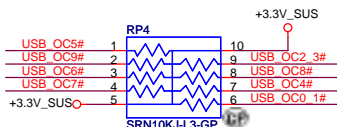
Layout Note:  
Place R563, R580 and R581  
within 500 mils from ICH.

### ICH8-Strap PIN

BOOT BIOS Strap		
PCI_GNT#0 (R617)	SPI_CS#1 (R623)	BOOT BIOS Location
0	1	SPI(Default)
1	0	PCI
1	1	LPC
A16 swap override strap		
PCI_GNT#3 (R620)	low = A16 swap override enable high = default	



### USB OC# PULL HIGH



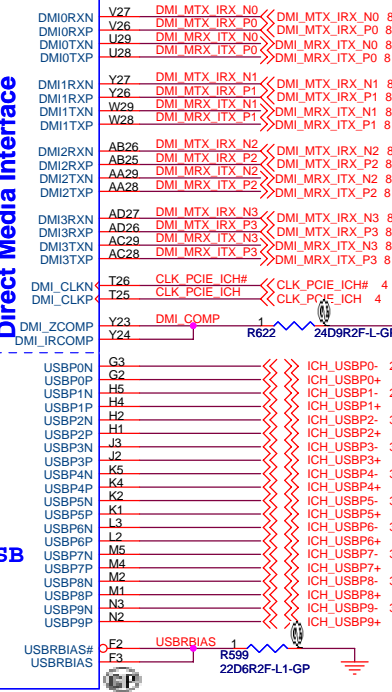
U39B 2 OF 6

### PCI-Express

### Direct Media Interface

### SPI

### USB

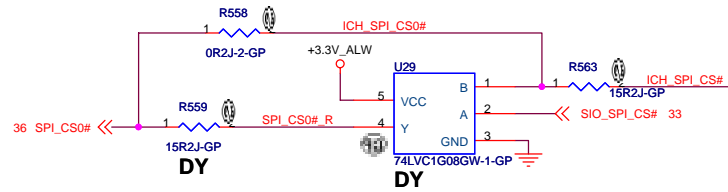


DMI\_COMP R622 place  
within 500 mil of ICH8M

### ICH

USB0	Ext Left Side
USB1	Ext Back
USB2	Ext Right Side (Top)
USB3	Ext Right Side (Bottom)
USB4	3rd mini card
USB5	Camera
USB6	Express Card
USB7	BT
USB8	Gaming LCD
USB9	WWAN

USBRBIAS close to ICH8M 500  
mils and Trace impedance  
should be 60 ohm +/- 15%

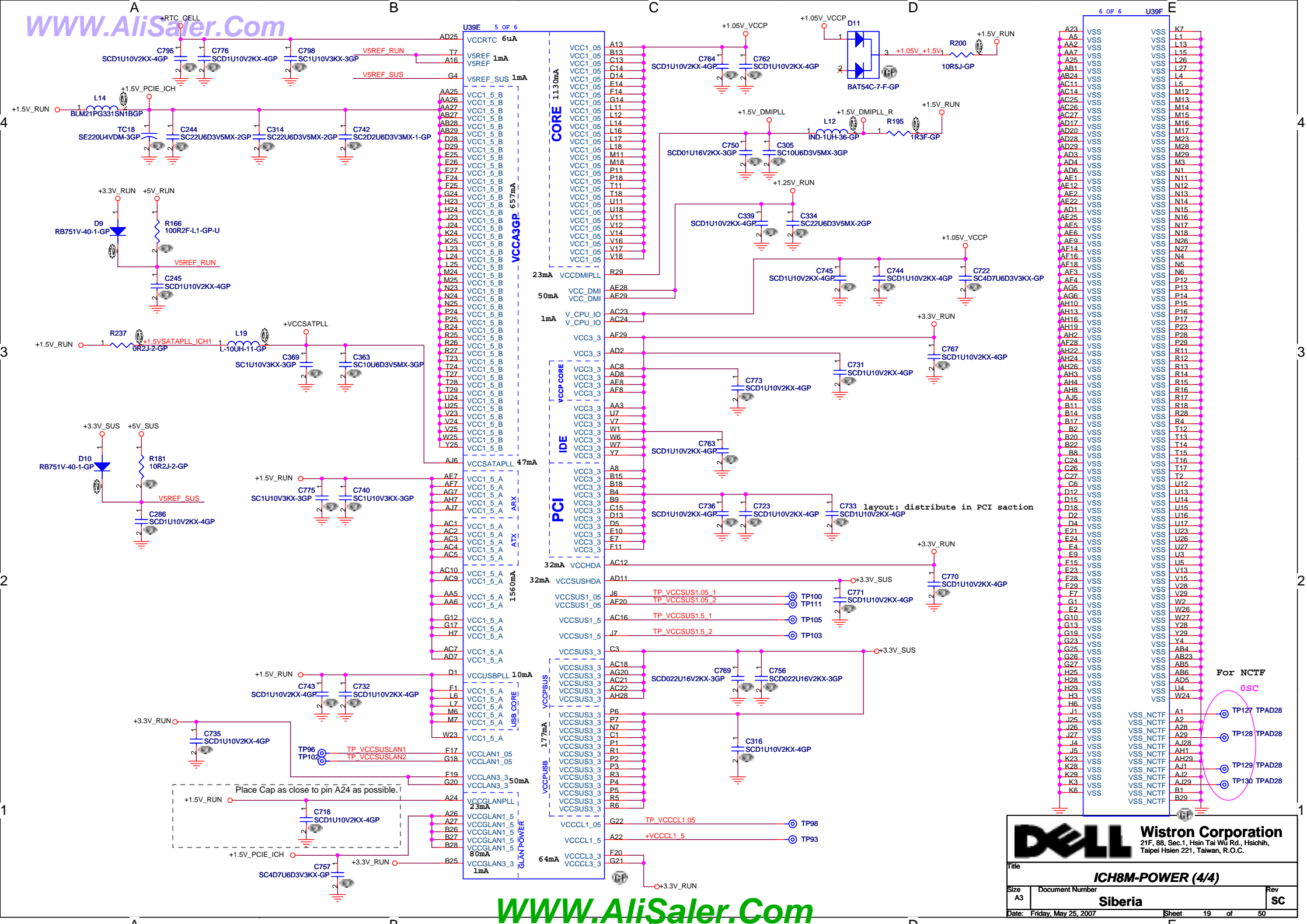


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Title <b>ICH8M-PCIE/USB/SPI/DMI (2/4)</b>		
Size A3	Document Number <b>Siberia</b>	Rev <b>SC</b>
Date: Friday, May 25, 2007	Sheet 17 of 50	







REM\_DIODE1\_N and REM\_DIODE1\_P  
routing Trace width and Spacing  
use 10 / 10 mil

Place inside CPU socket

Locate C586 near Guardian

H\_THERMDA and H\_THERMDC  
routing Trace width and  
Spacing use 10 / 10 mil

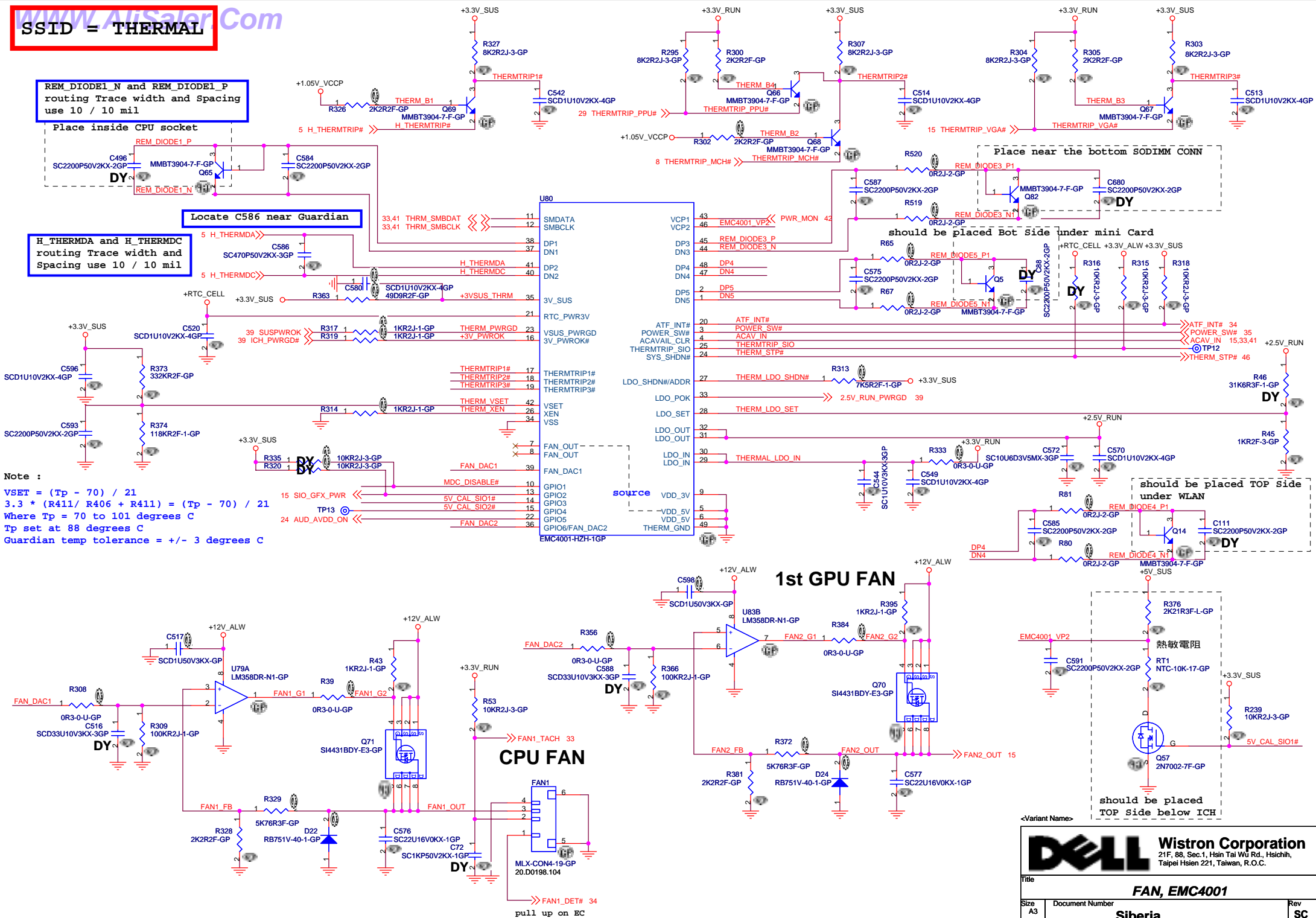
should be placed Bot Side under mini Card

should be placed TOP Side under WLAN

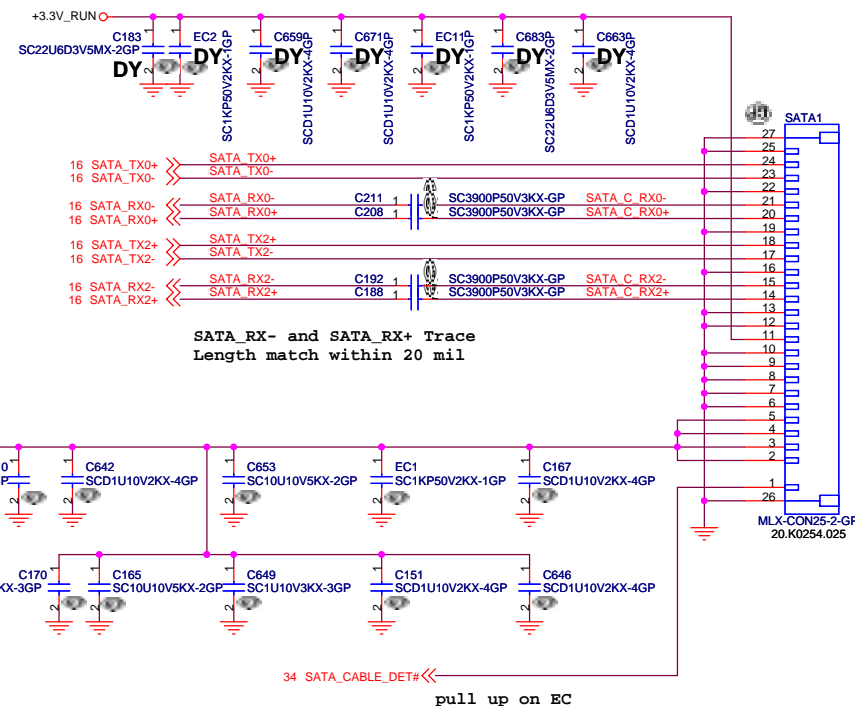
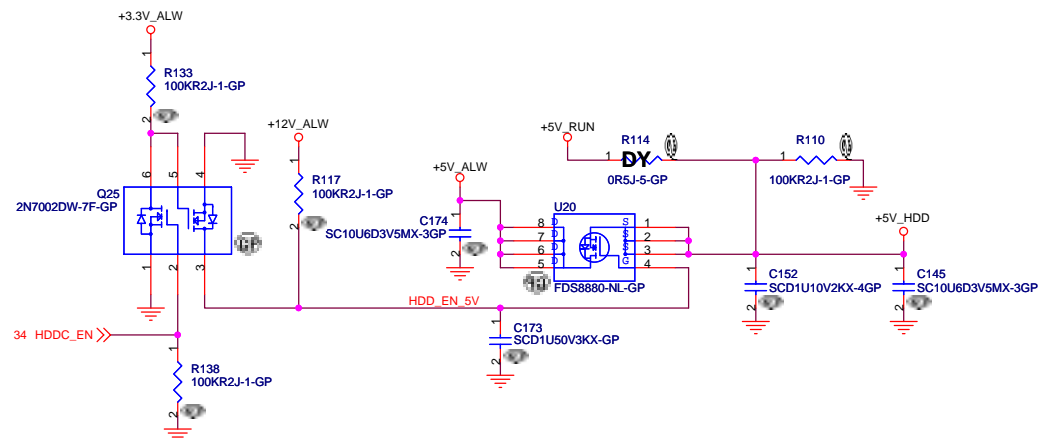
should be placed TOP side below ICH

Note :

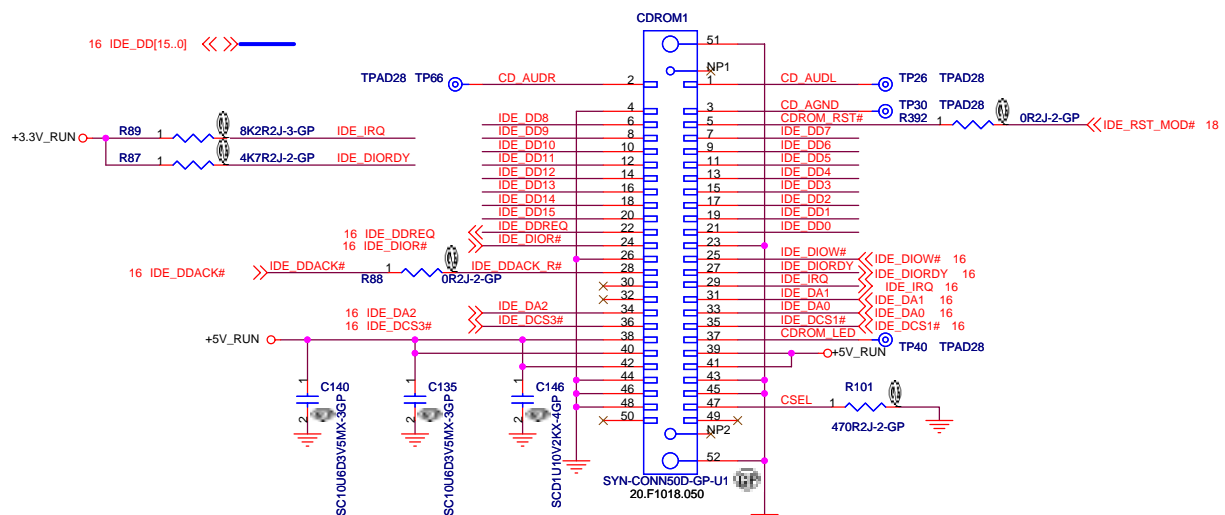
$VSET = (T_p - 70) / 21$   
 $3.3 * (R411 / R406 + R411) = (T_p - 70) / 21$   
 Where  $T_p = 70$  to  $101$  degrees C  
 $T_p$  set at  $88$  degrees C  
 Guardian temp tolerance =  $\pm 3$  degrees C



## SATA HDD Connector



## ODD Connector



<Variant Name>



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Taipei Hsien 221, Taiwan, R.O.C.

Title

***HDD&ODD***Size  
A2

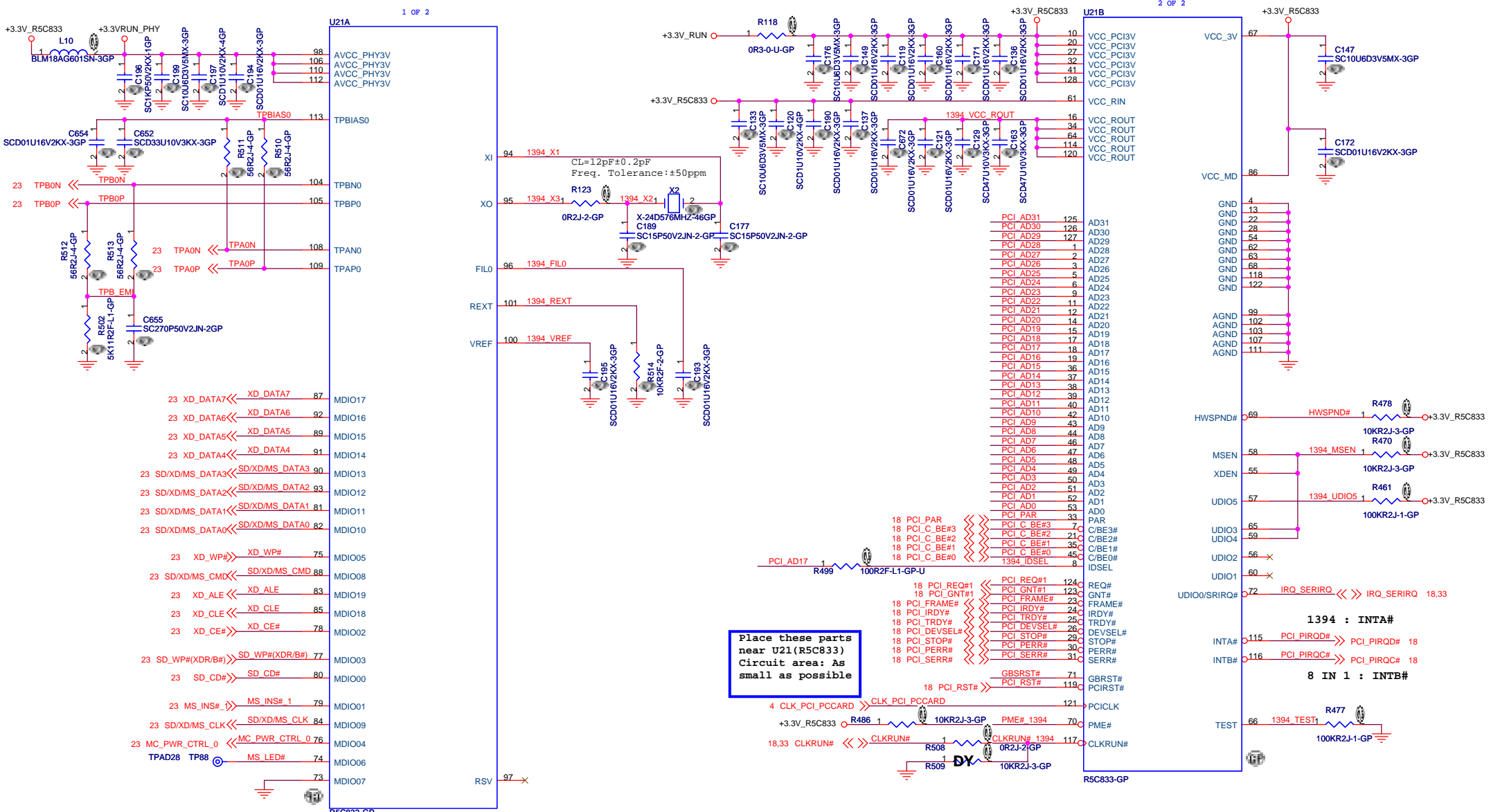
	Document Number
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## Siberia

Rev	SC
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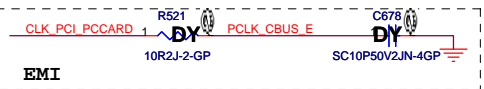
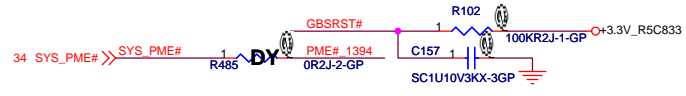
Date: Friday, May 25, 2007

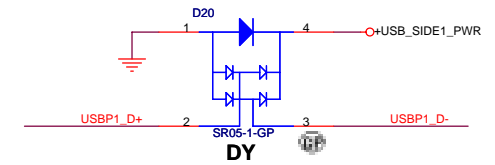
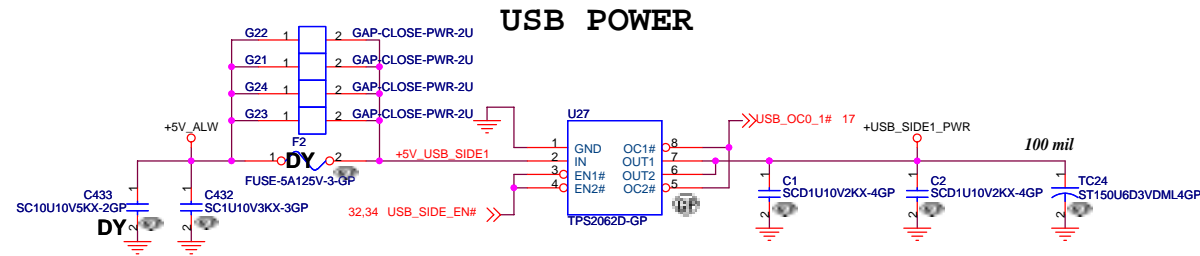
Sheet 21 of 5



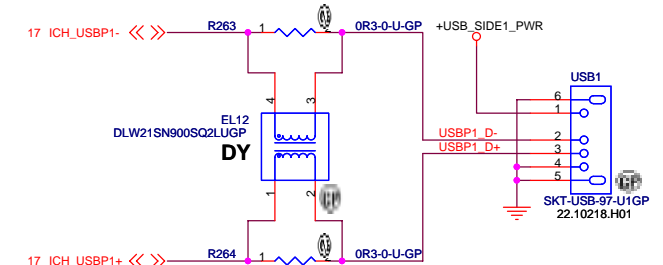
We use the R5C832 in X00 for R5C833 not ready.

SSID = 1394



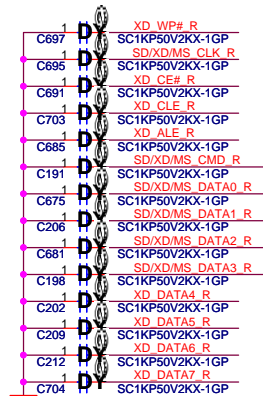
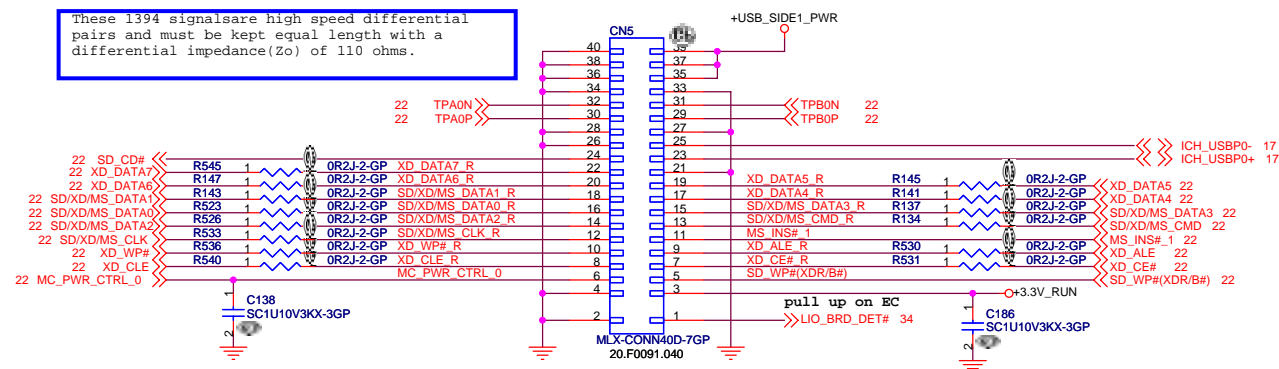


Place ESD diodes as close to the connector as passible.



**I/O board conn. (1394/7 IN 1/USB)**

These 1394 signals are high speed differential pairs and must be kept equal length with a differential impedance ( $Z_o$ ) of 110 ohms.



**<Variant Name>**

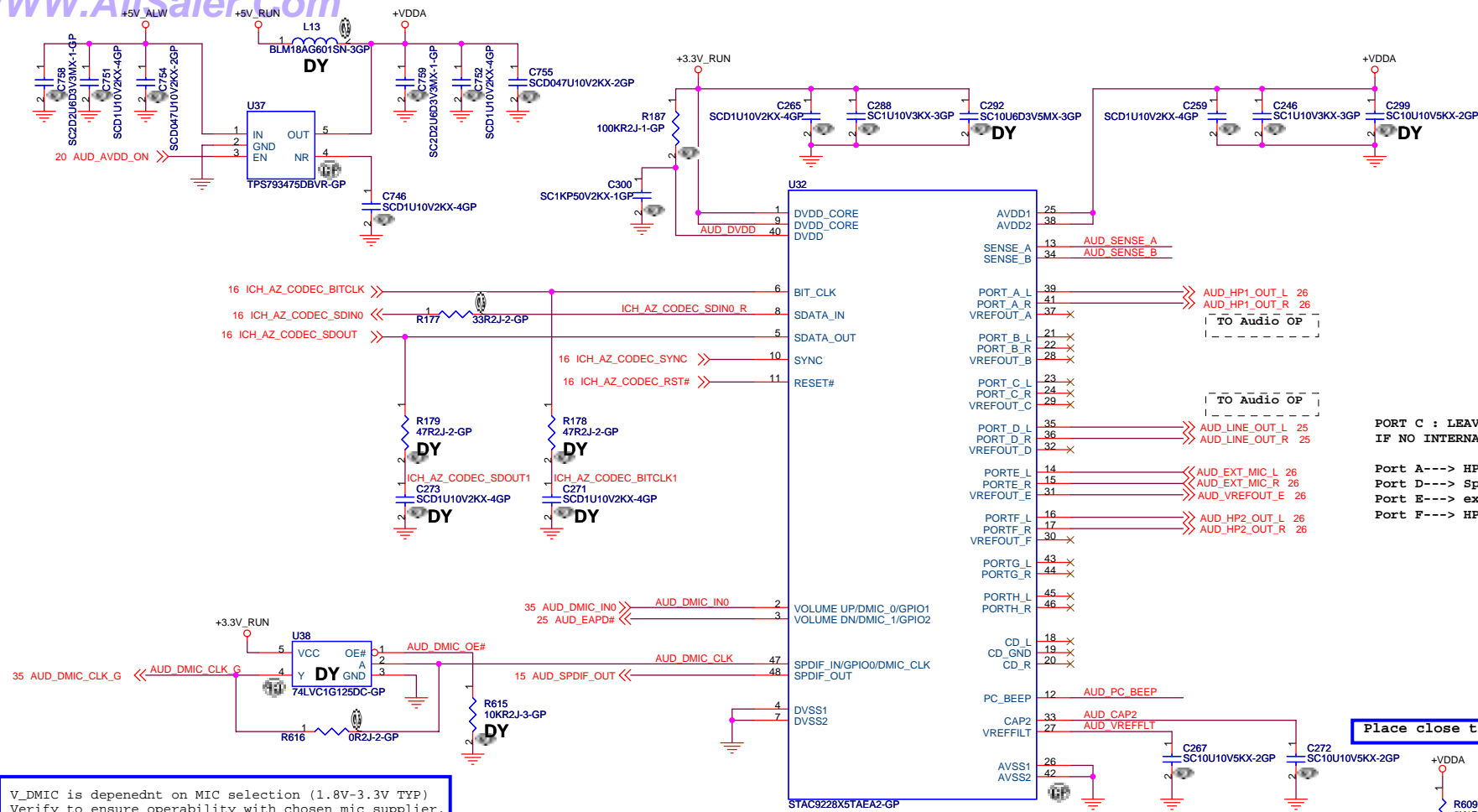


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,  
Taipei Hsien 221, Taiwan, R.O.C.

Title	<b>I/O board (1394/7 IN 1/USB) / USB CONN.</b>
-------	--

Size A3	Document Number <b>Siberia</b>	Rev <b>SC</b>
Date: Friday, May 25, 2007	Sheet 23 of 50	

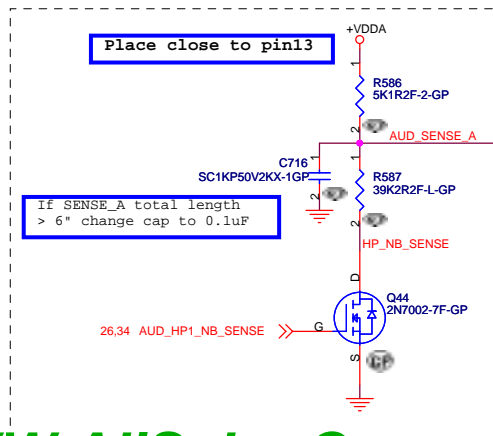
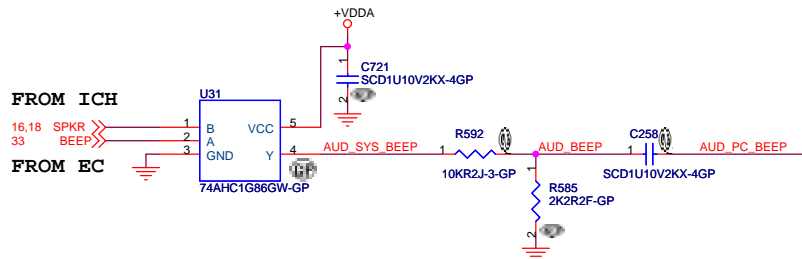




PORT C : LEAVE NC  
IF NO INTERNAL MICS.

Port A--> HP1  
Port D--> Speaker  
Port E--> ext Mic  
Port F--> HP2

V\_DMIC is depenednt on MIC selection (1.8V-3.3V TYP)  
Verify to ensure operability with chosen mic supplier.  
Note1: If only 1 digital mic, use AUD\_DMIC\_IN0.  
Note2: If using 2 digital mics, also use AUD\_DMIC\_IN0.  
This input supports 2 digital mics.  
AUD\_DMIC\_IN1 is only used to support 4 digital mics.



If SENSE\_B total length  
> 6" change cap to 0.1uF

Place close to pin34

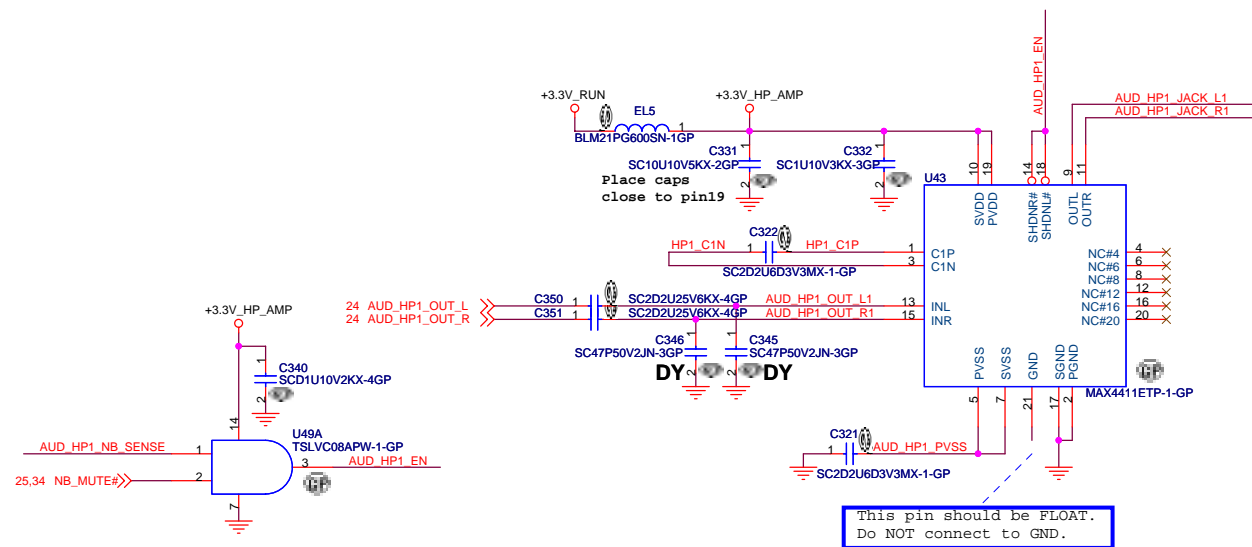
<Variant Name>

**DELL Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

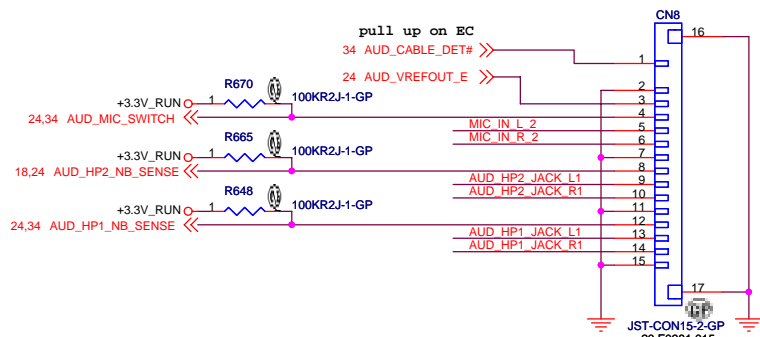
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Size	Document Number		Siberia		Rev
A3					SC
Date:	Friday, May 25, 2007		Sheet	24	of 50



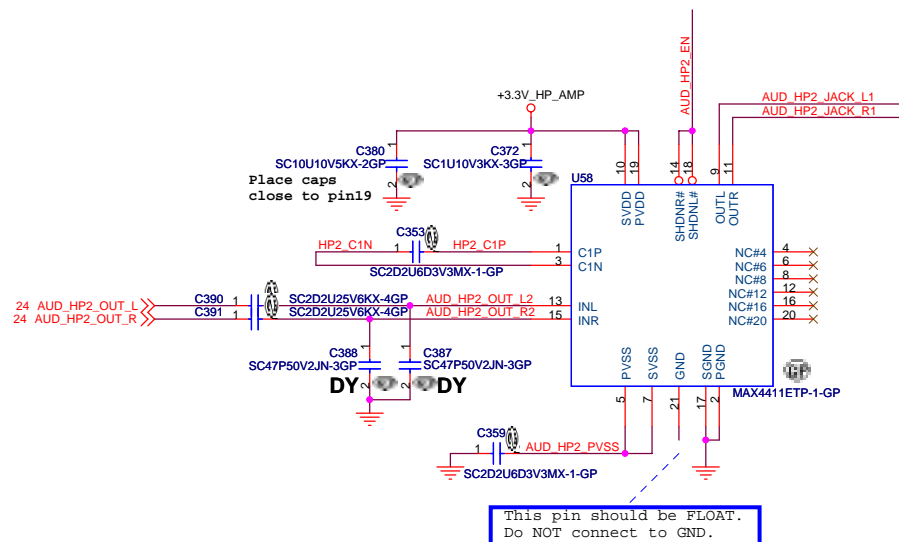
## Head Phone 1



## MIC



## Head Phone 2



<Core Design>

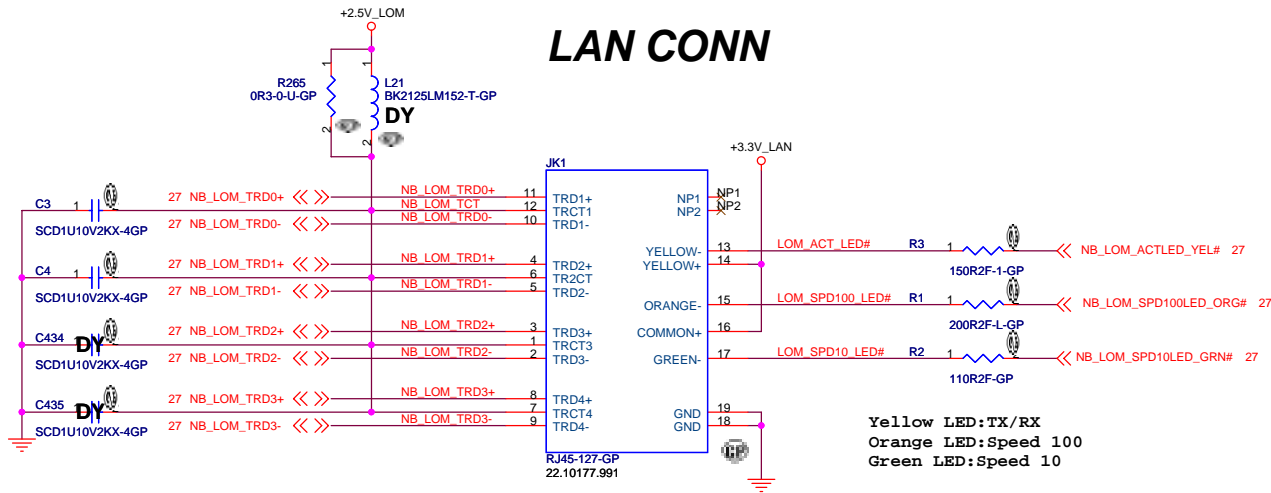
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title **AUDIO (3/3)**

Size A3 Document Number **Siberia** Rev **SC**

Date: Friday, May 25, 2007 Sheet 26 of 50



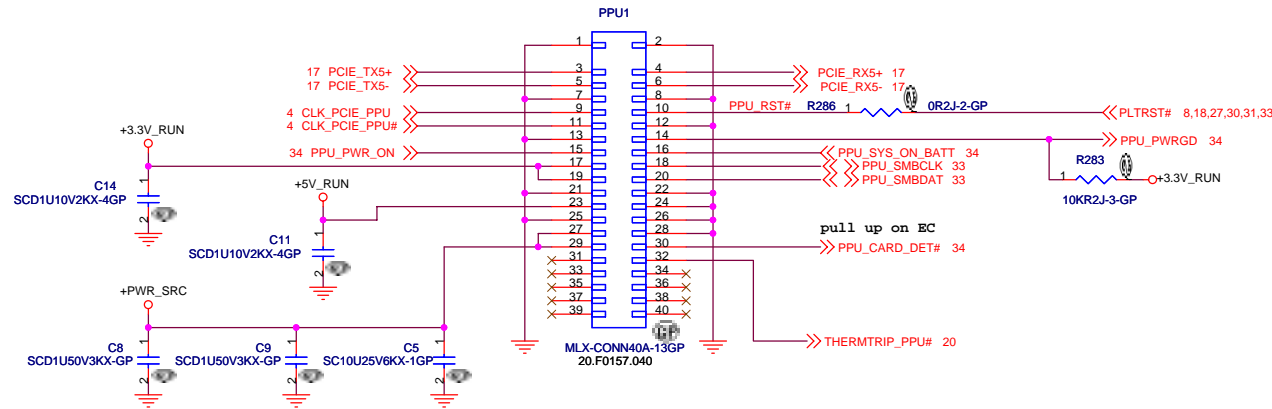


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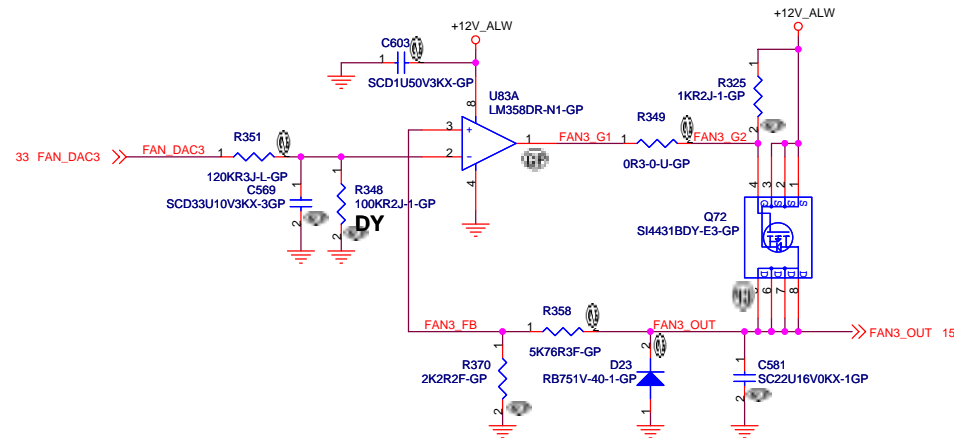
<b>DELL</b>		<b>Wistron Corporation</b> 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title <b>LAN Connector</b>			
Size A3	Document Number <b>Siberia</b>	Rev <b>SC</b>	
Date: Friday, May 25, 2007	Sheet 28 of 50		



## PPU connector



## 2nd GPU FAN

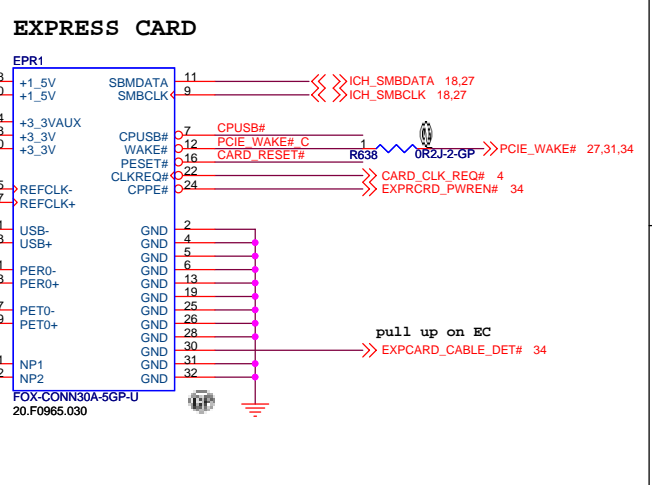
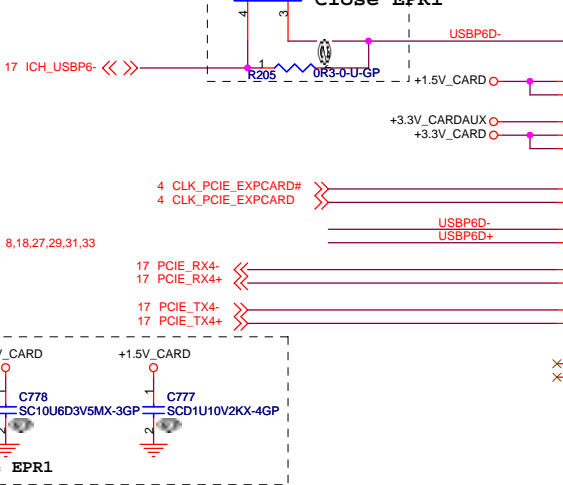
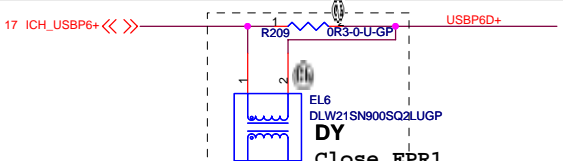
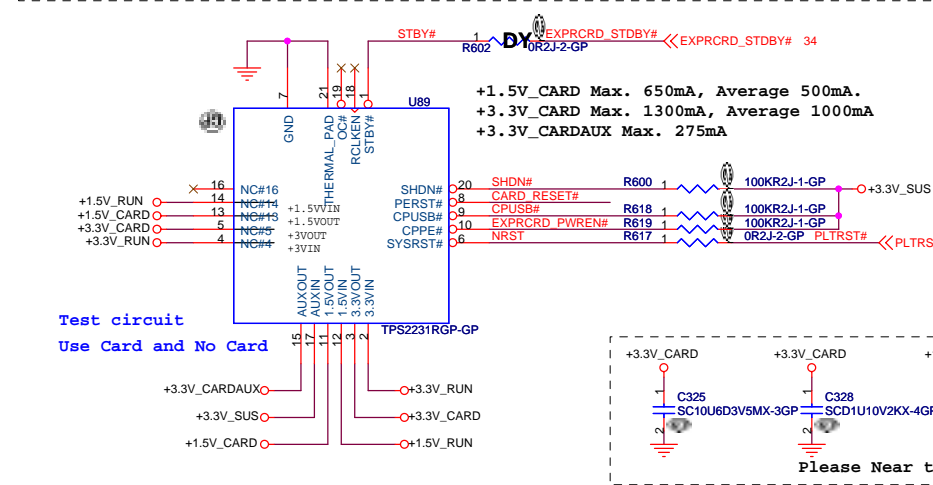
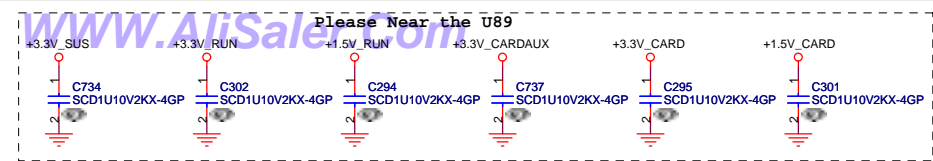


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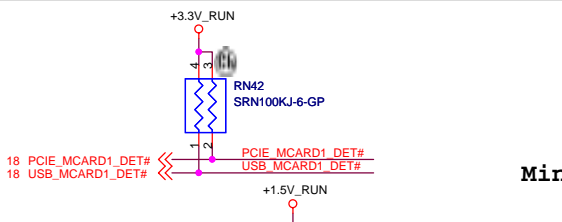
**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		PPU CONN. / 2rd GPU FAN	
Size	Document Number	Rev	SC
A3	Siberia		
Date:	Friday, May 25, 2007	Sheet	29 of 50

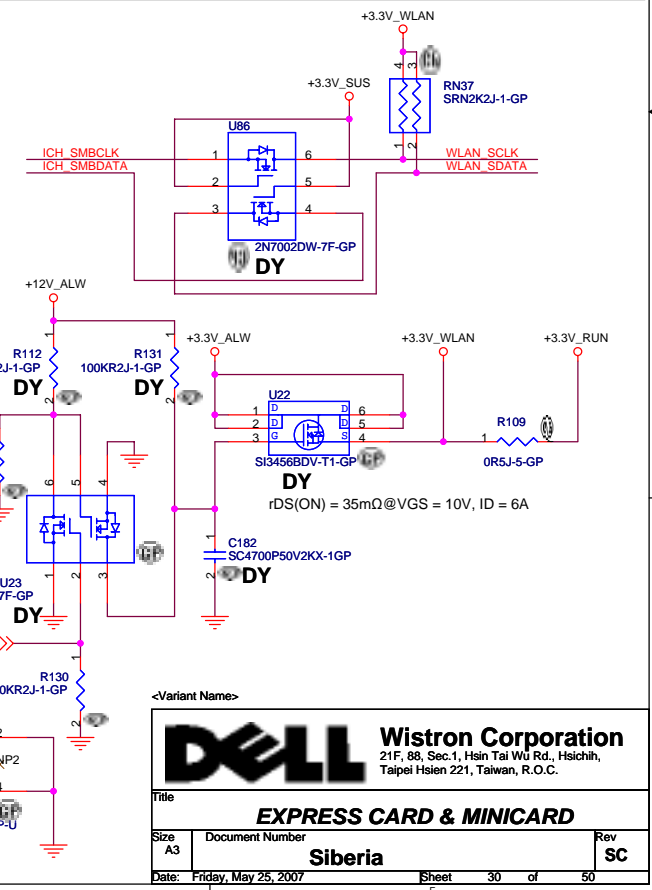
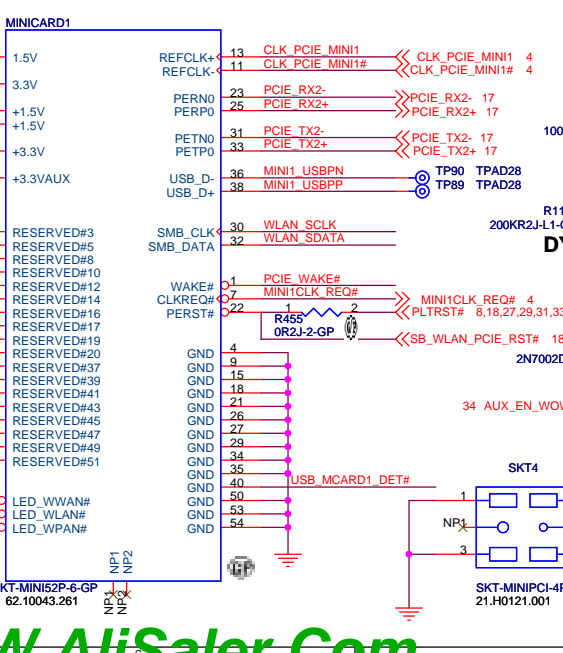
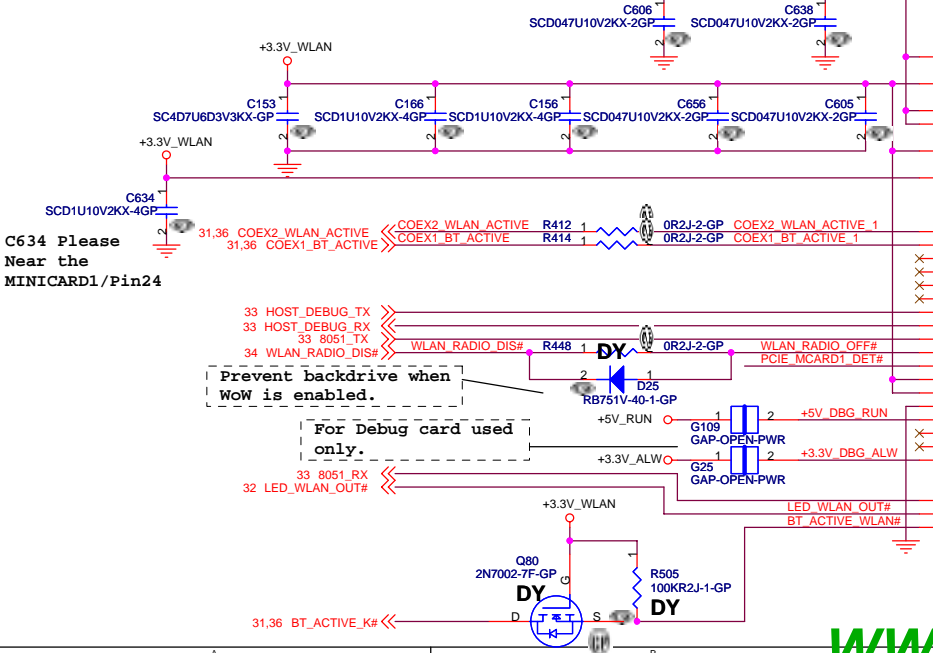


**DEBUG PINS**

JMINI Pin	Debug Pin Name	EC Pin
16	HOST_DEBUG_TX	70
17	HOST_DEBUG_RX	71
19	8051_TX	82
42	8051_RX	81



**MiniCard WLAN connector**

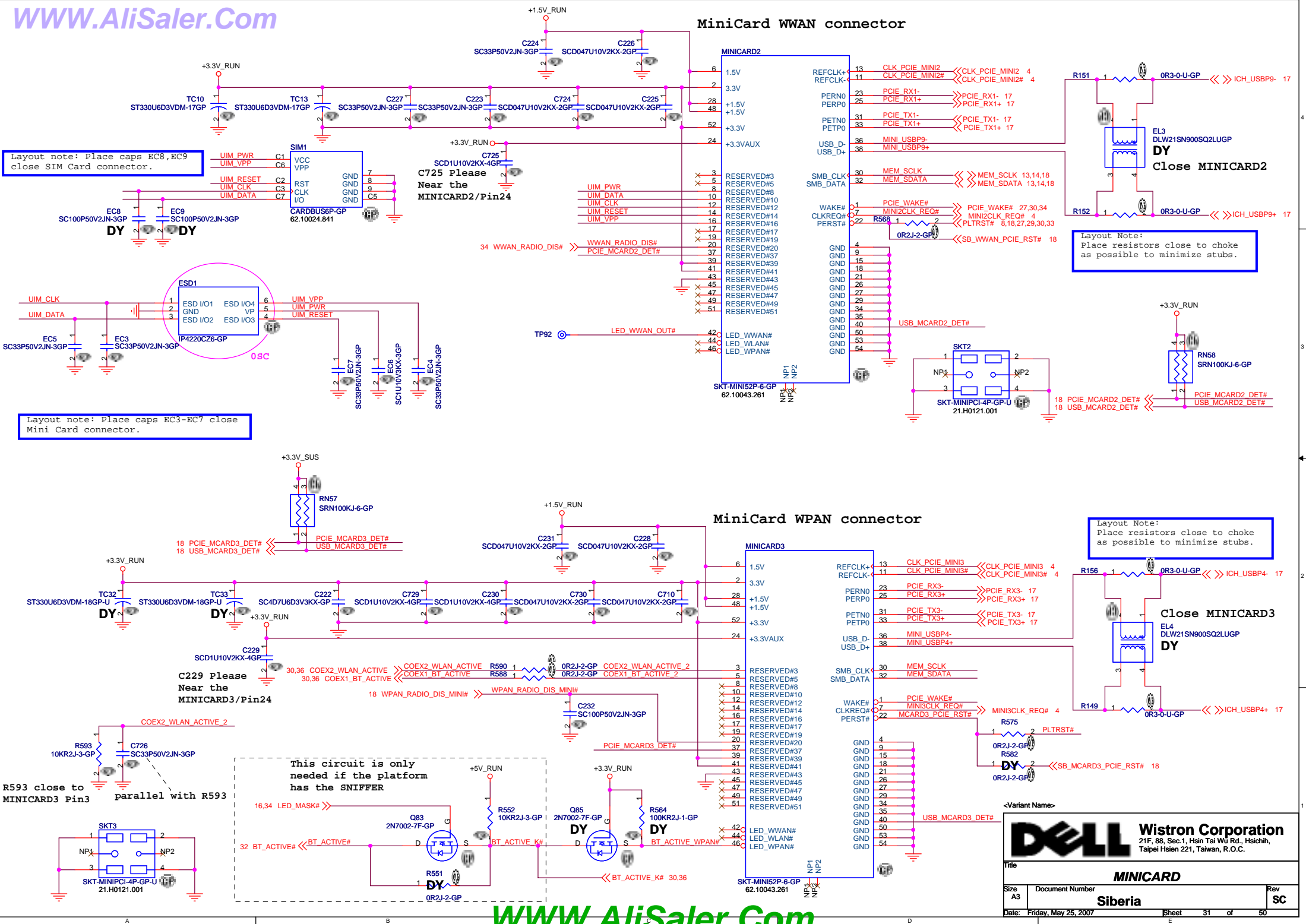


**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

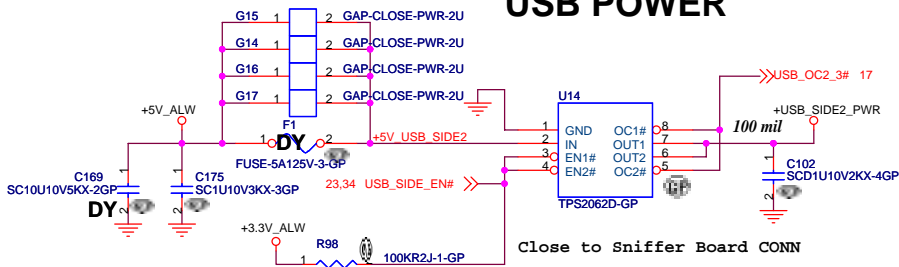
**EXPRESS CARD & MINICARD**

Size A3 Document Number Siberia Rev SC

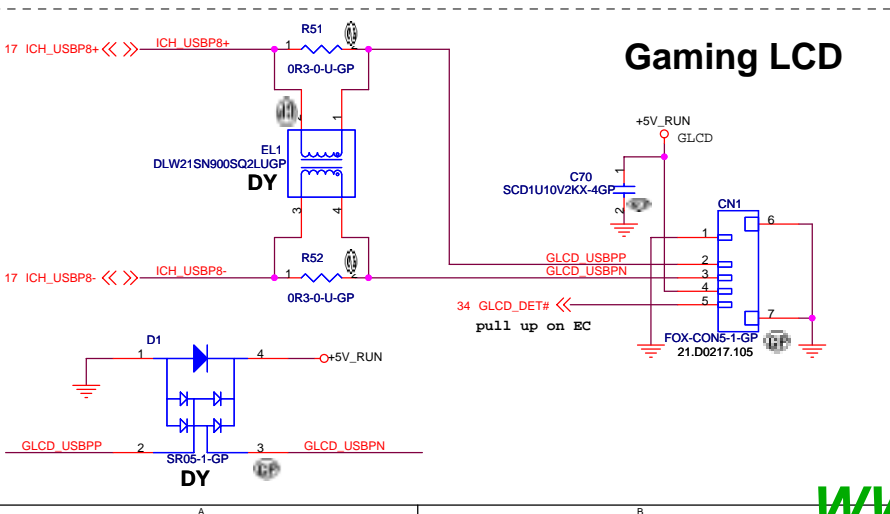
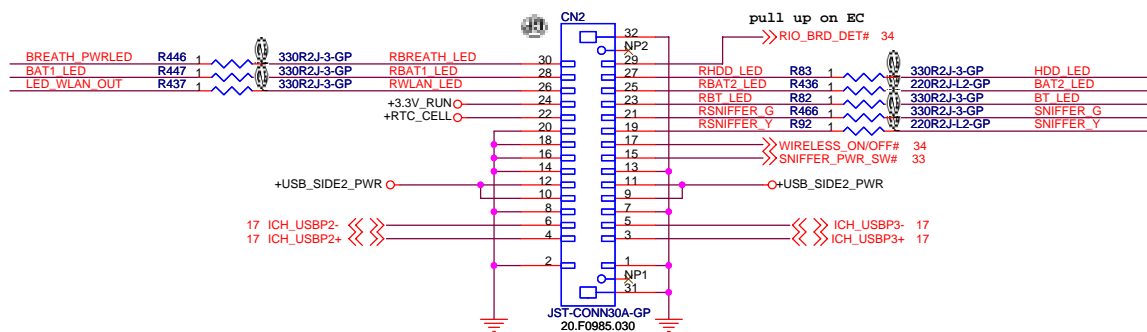
Date: Friday, May 25, 2007 Sheet 30 of 50



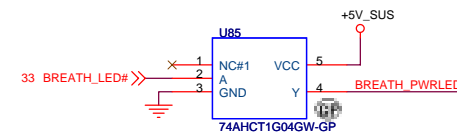
## USB POWER



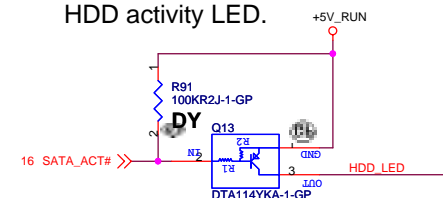
## Sniffer board for USB, Indicator LEDs, Sniffer Switch conn.



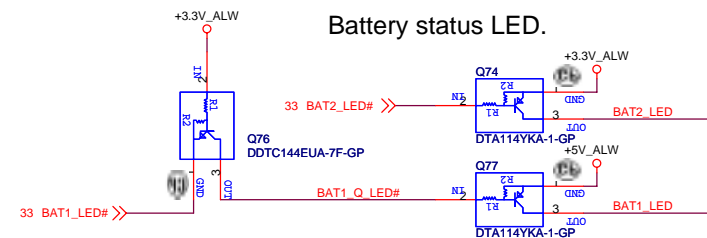
## Power & Suspend LED.



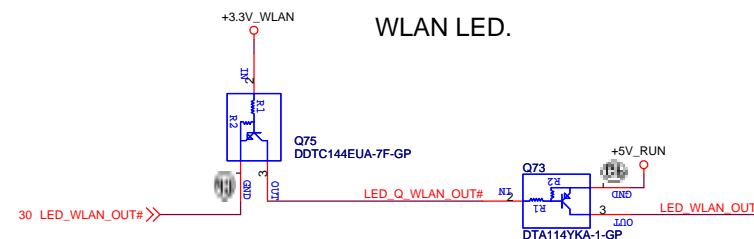
## HDD activity LED.



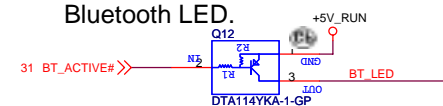
## Battery status LED.



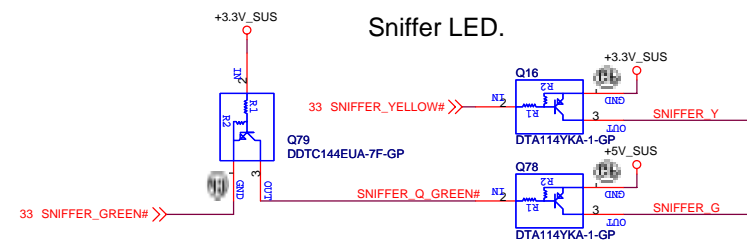
## WLAN LED.



## Bluetooth LED.



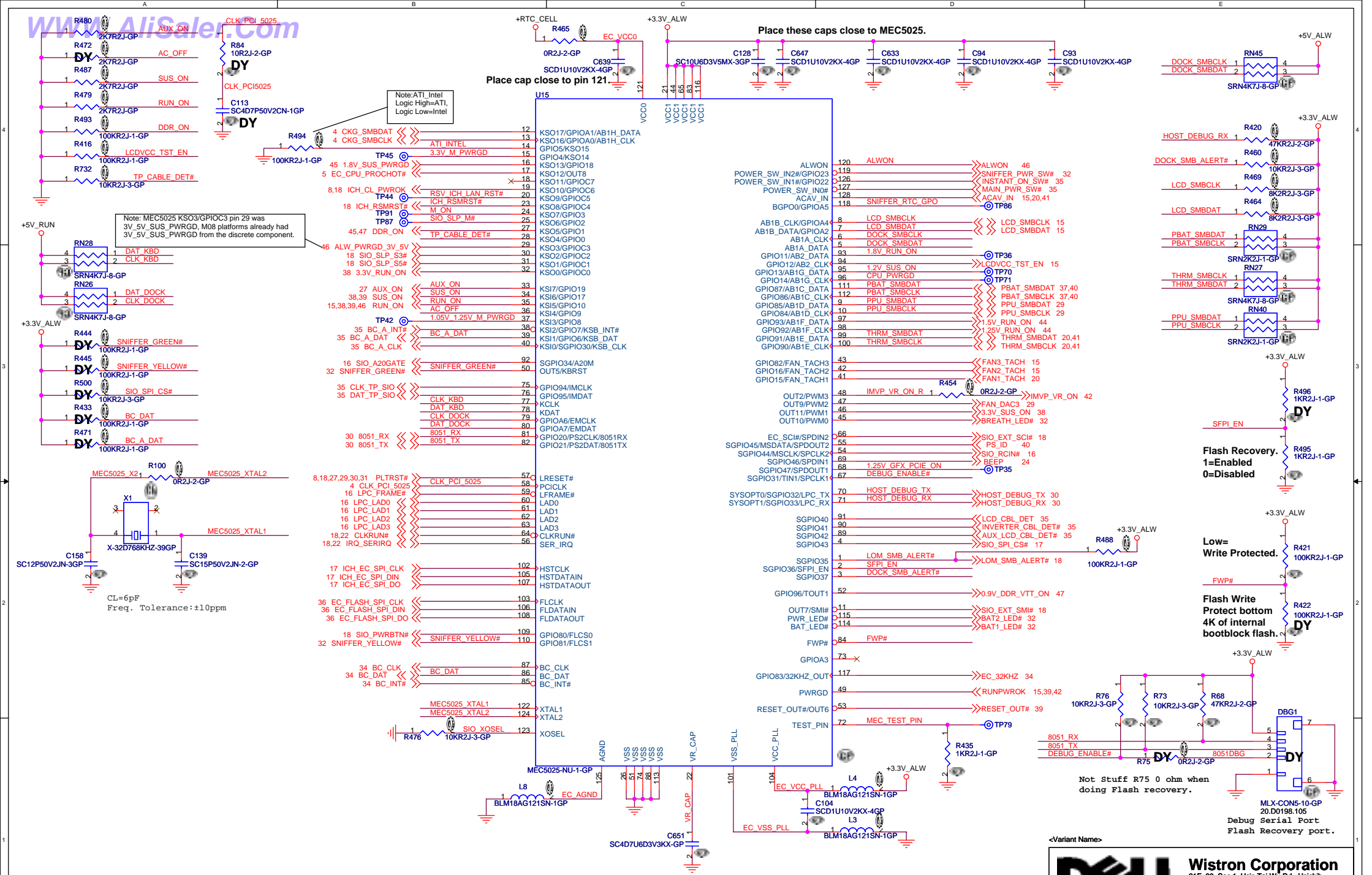
## Sniffer LED.



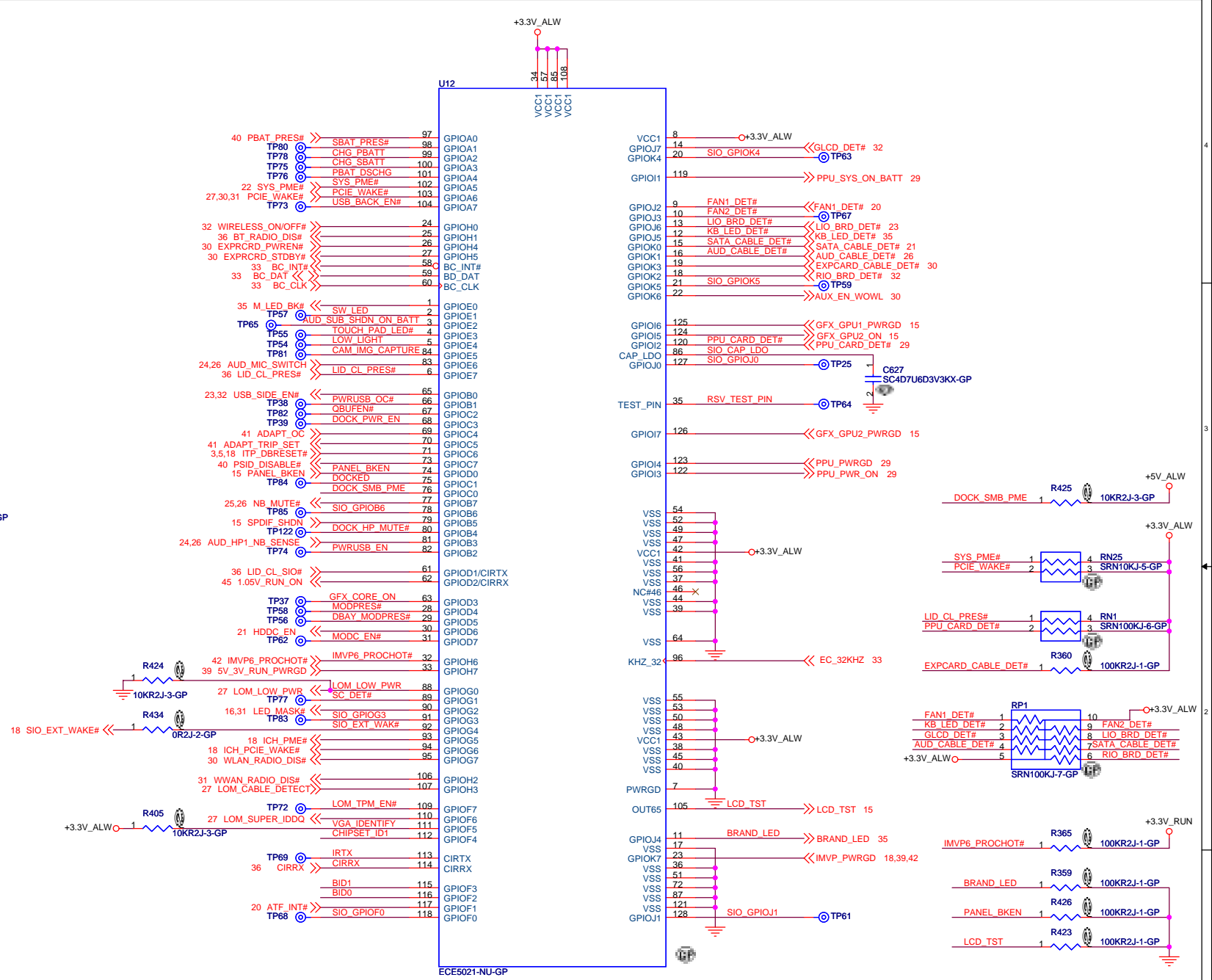
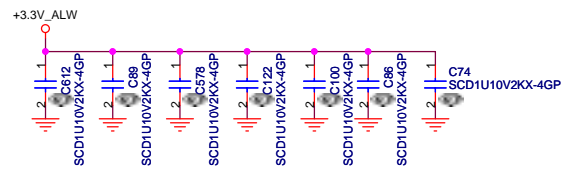
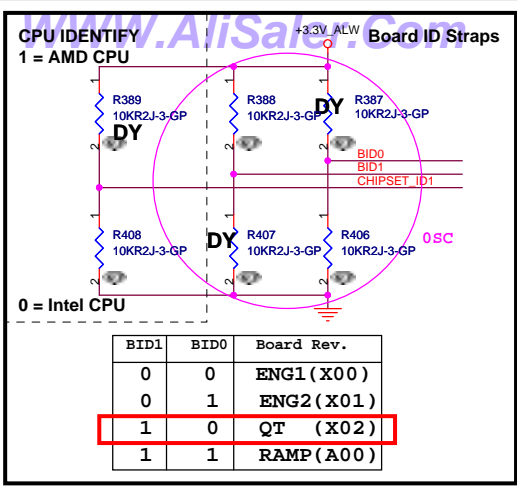
<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title		Sniffer board (USB/Status LEDs) / Gaming LCD	
Size	A3	Document Number	Siberia
Date:	Friday, May 25, 2007	Sheet	32 of 50
		Rev	SC







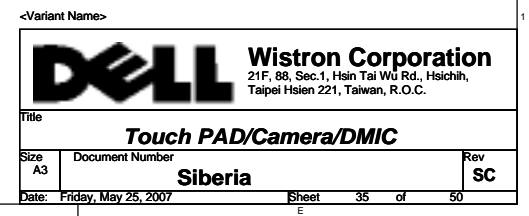
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**Wistron Corporation**  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

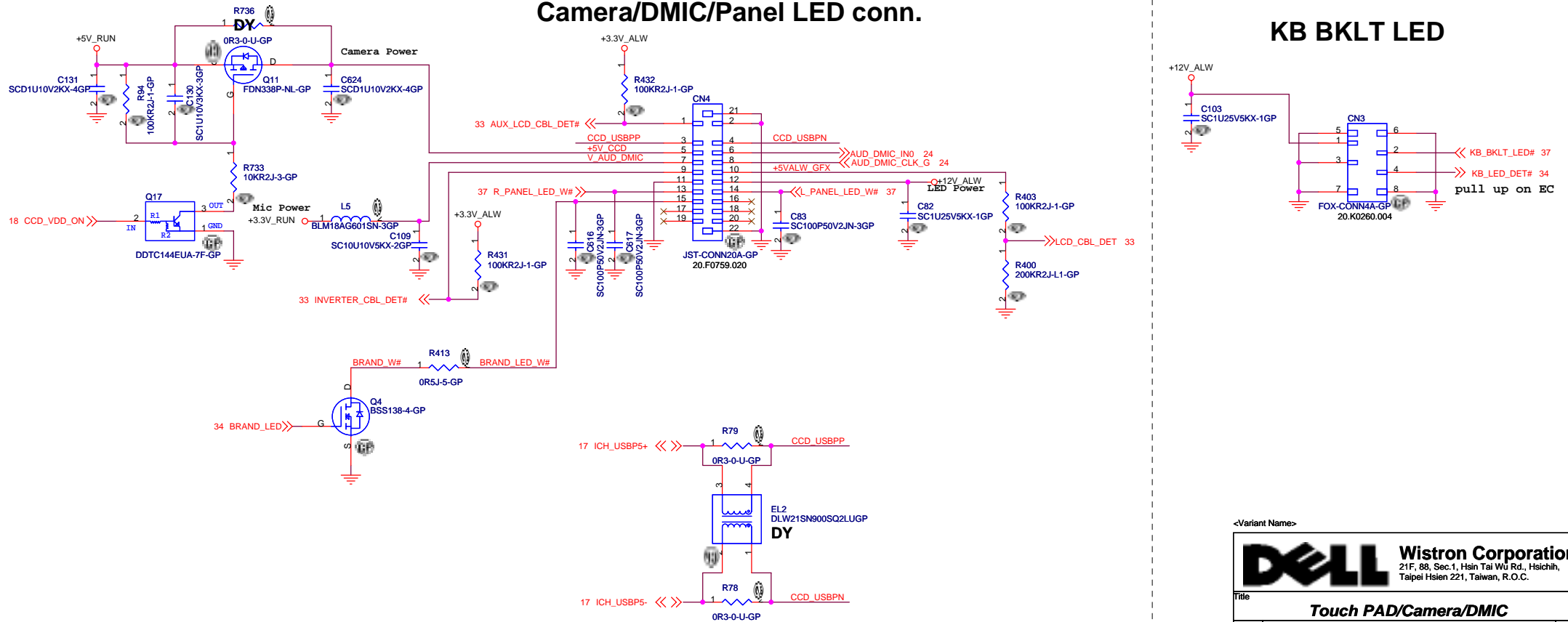
Title: **SIO ECE5021**

Size A3	Document Number	Rev SC
Date: Friday, May 25, 2007	Siberia	Sheet 34 of 50

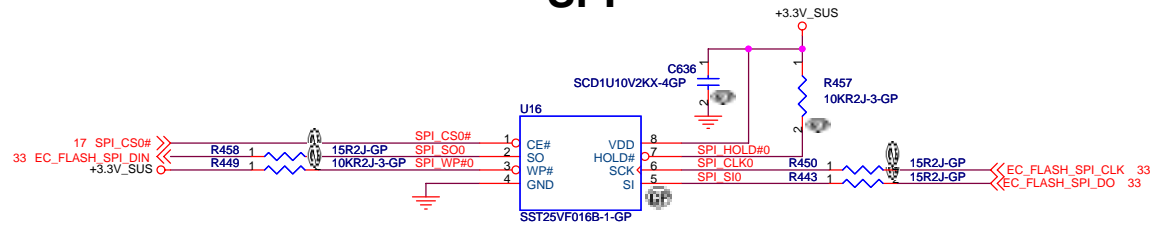
**WWW.AliSaler.Com**



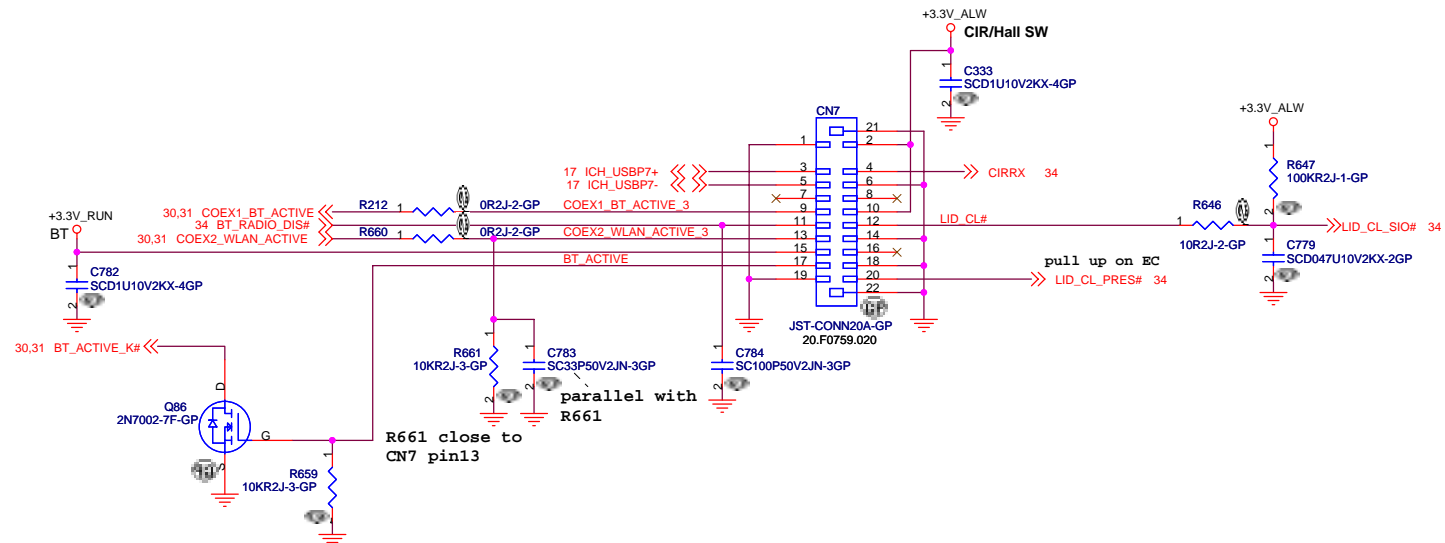
## KB BKLT LED



## SPI



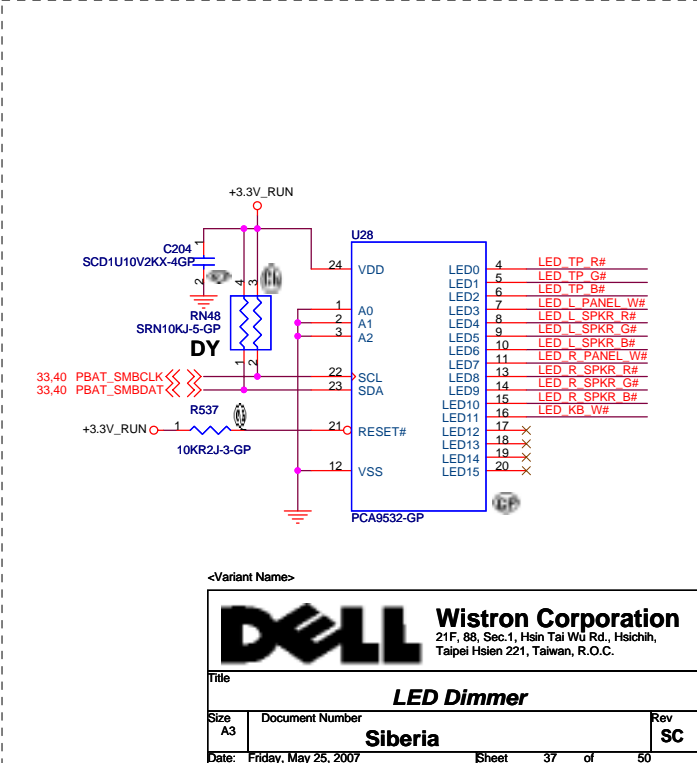
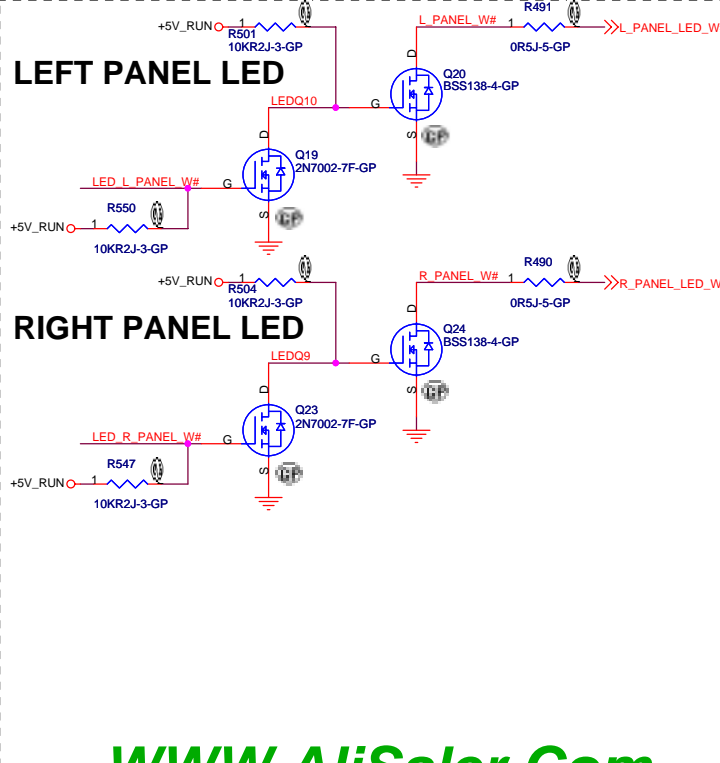
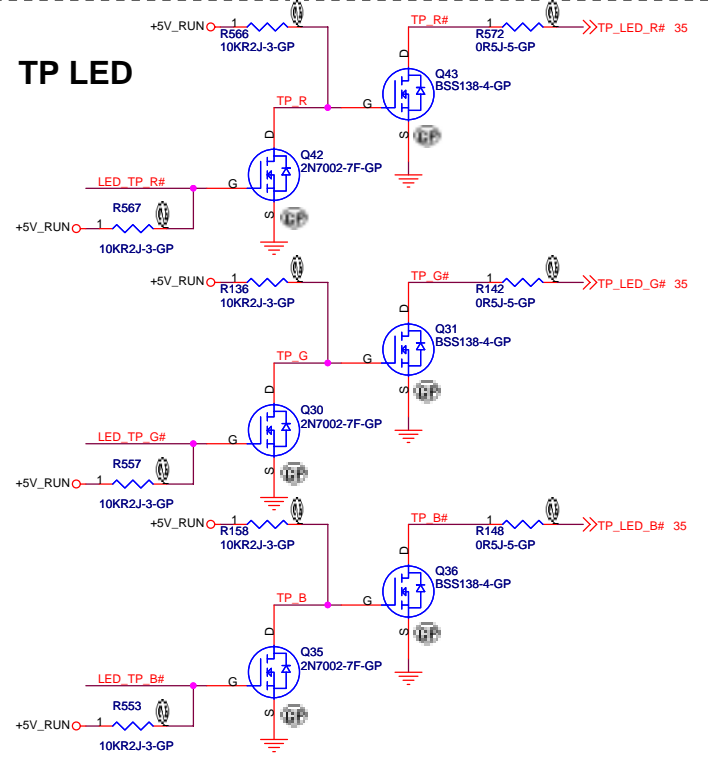
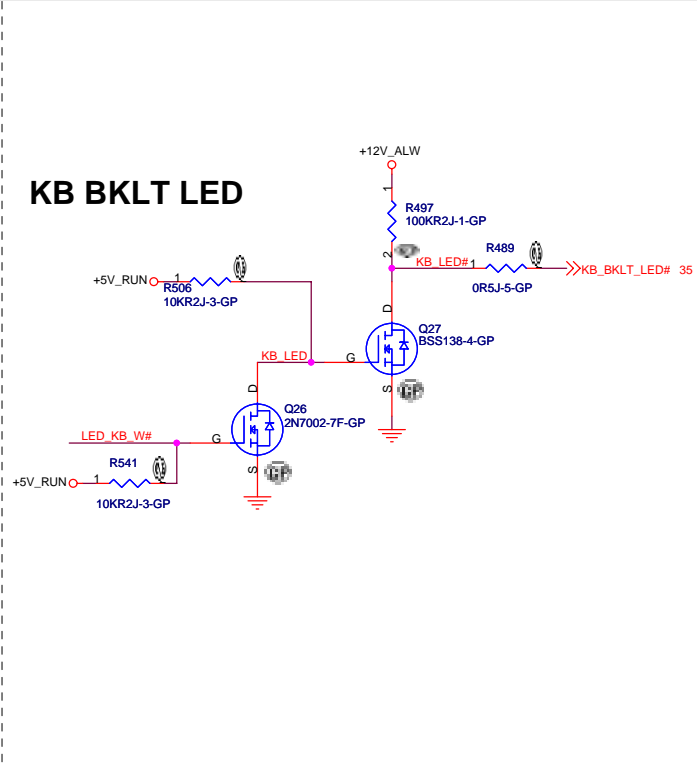
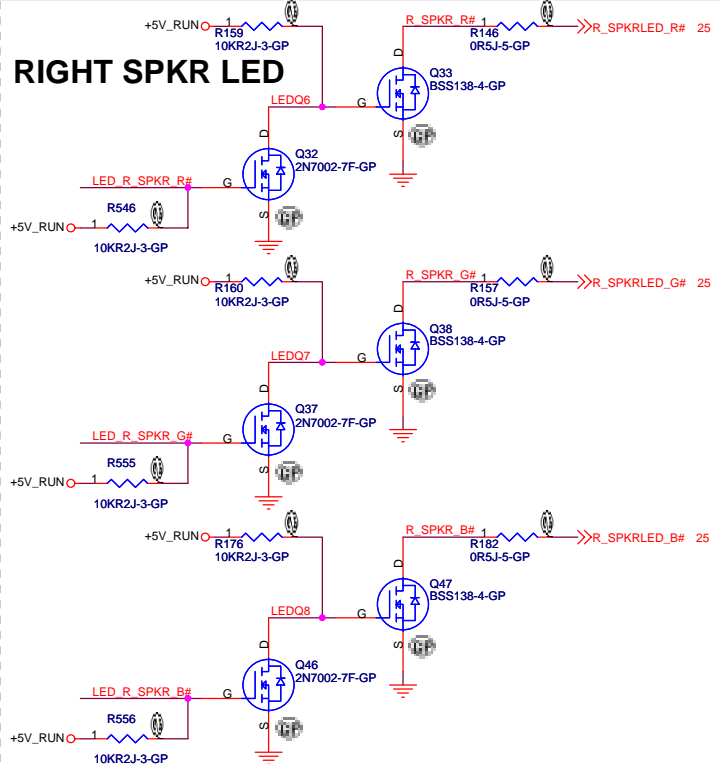
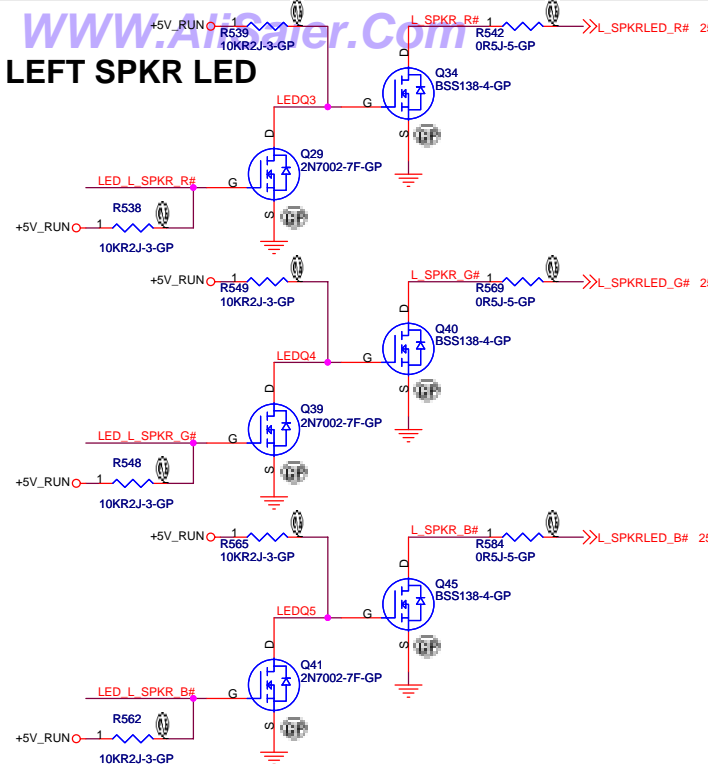
## Bluetooth/ CIR/ Hall SW



<Variant Name>



Title			SPI FLASH / Bluetooth / CIR / LID	
Size	Document Number	Siberia		Rev
A3				SC
Date:	Friday, May 25, 2007	Sheet	36	of 50



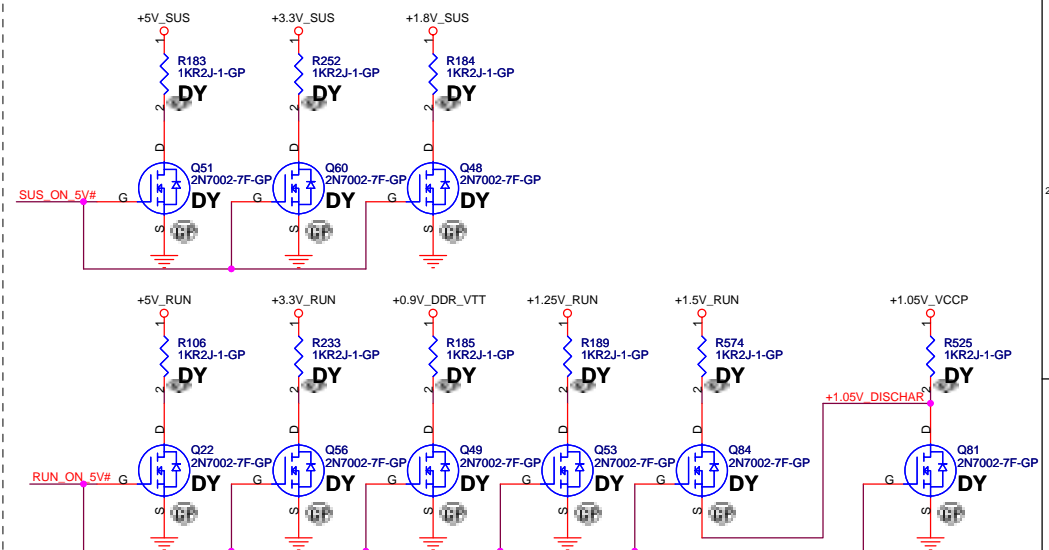
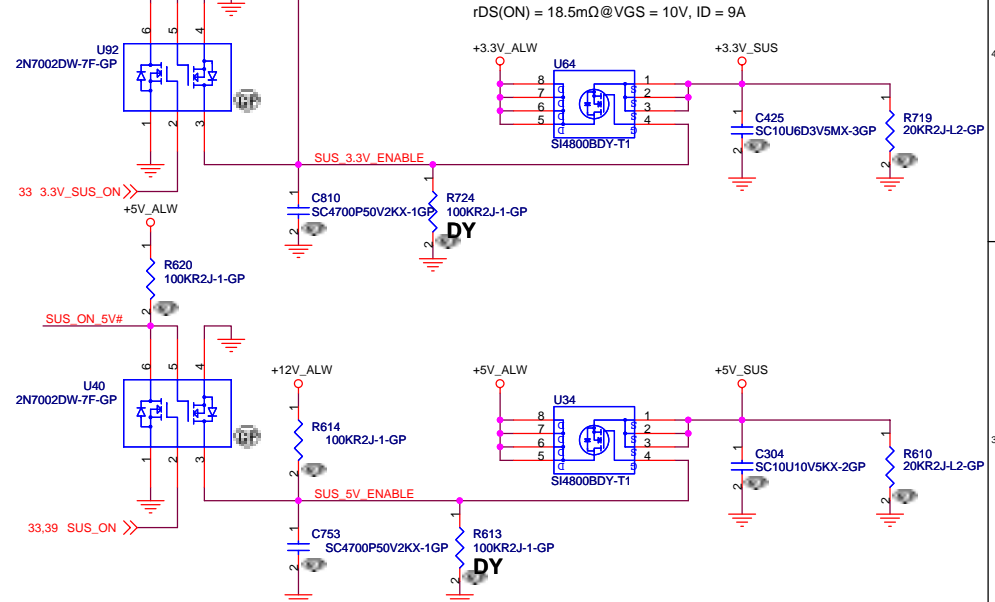
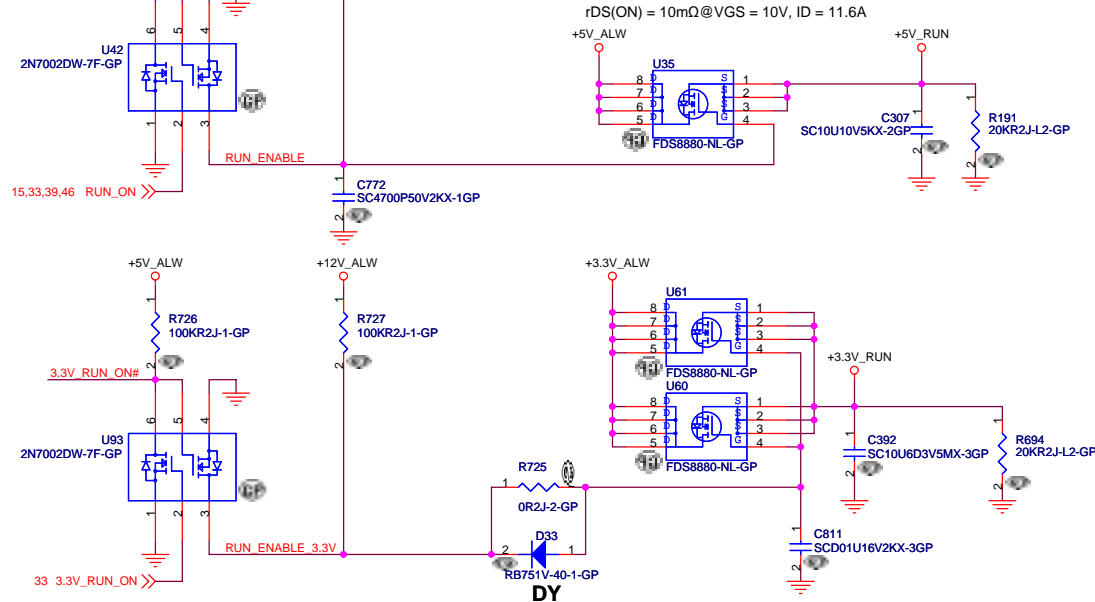
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**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LED Dimmer**

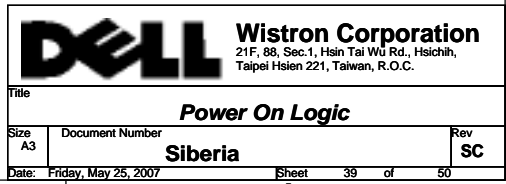
Size: A3 Document Number: **Siberia** Rev: **SC**

Date: Friday, May 25, 2007 Sheet: 37 of 50



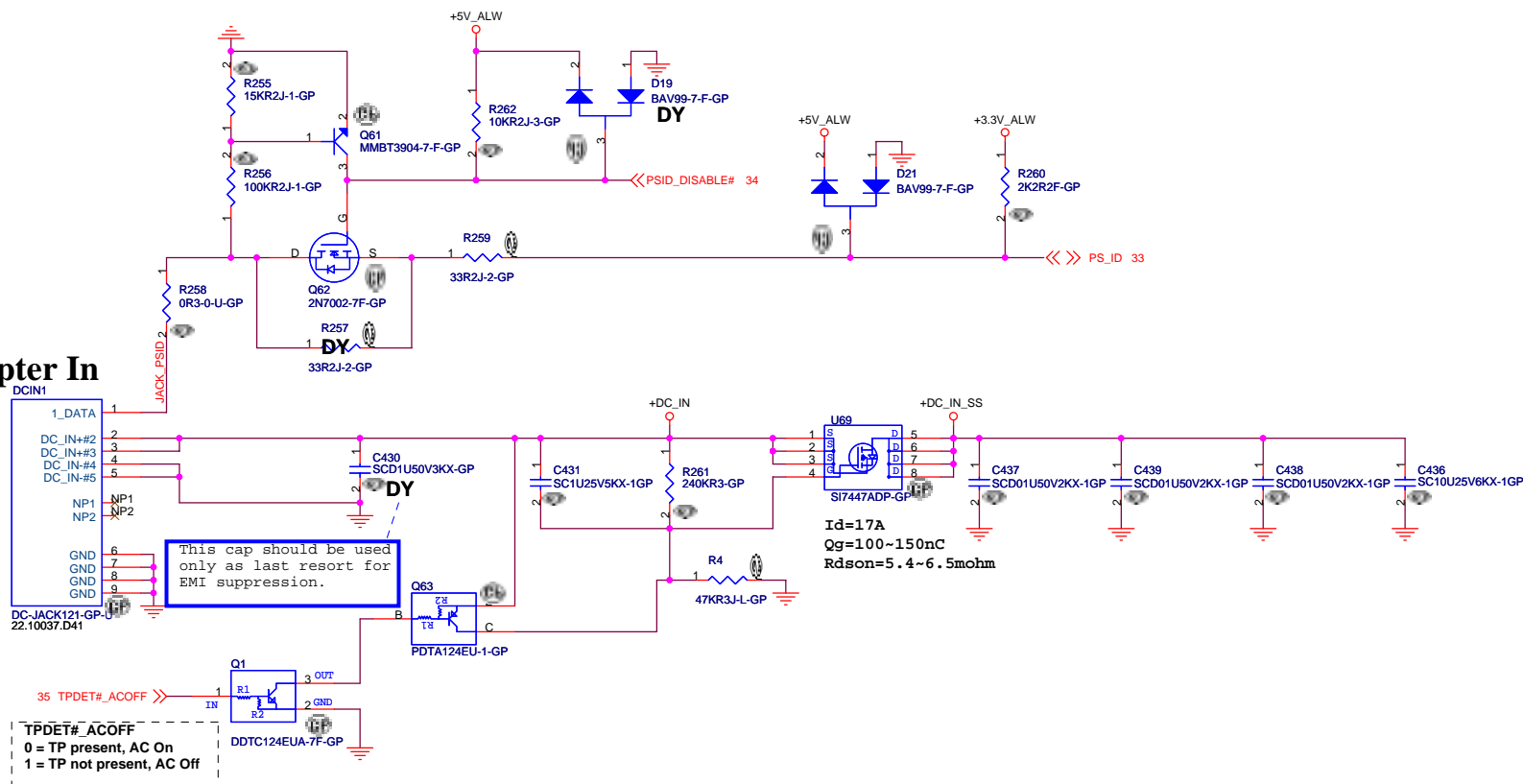
### Reserve discharge path

CRB 0.95:  
Insures that +1.05\_VCCP and +1.5\_RUN ramp down together by discharging +1.5V\_RUN into +1.05V\_VCCP

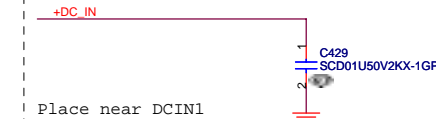




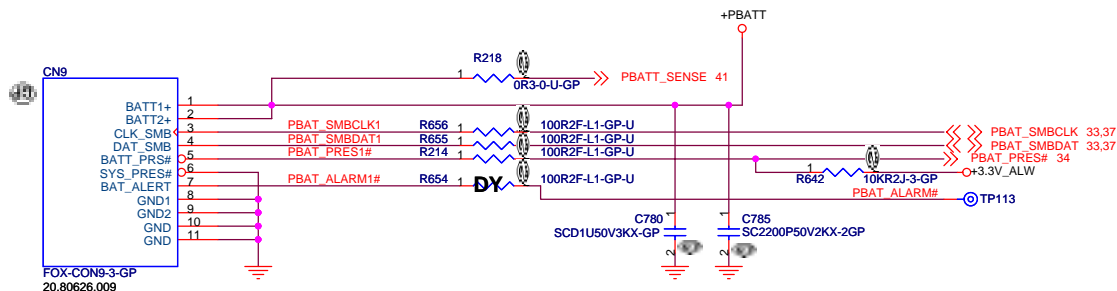
## Adapter In



## Reserved for EMI



## Batt Connector



<Variant Name>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

Title  
**DCIN / BATT CONN.**

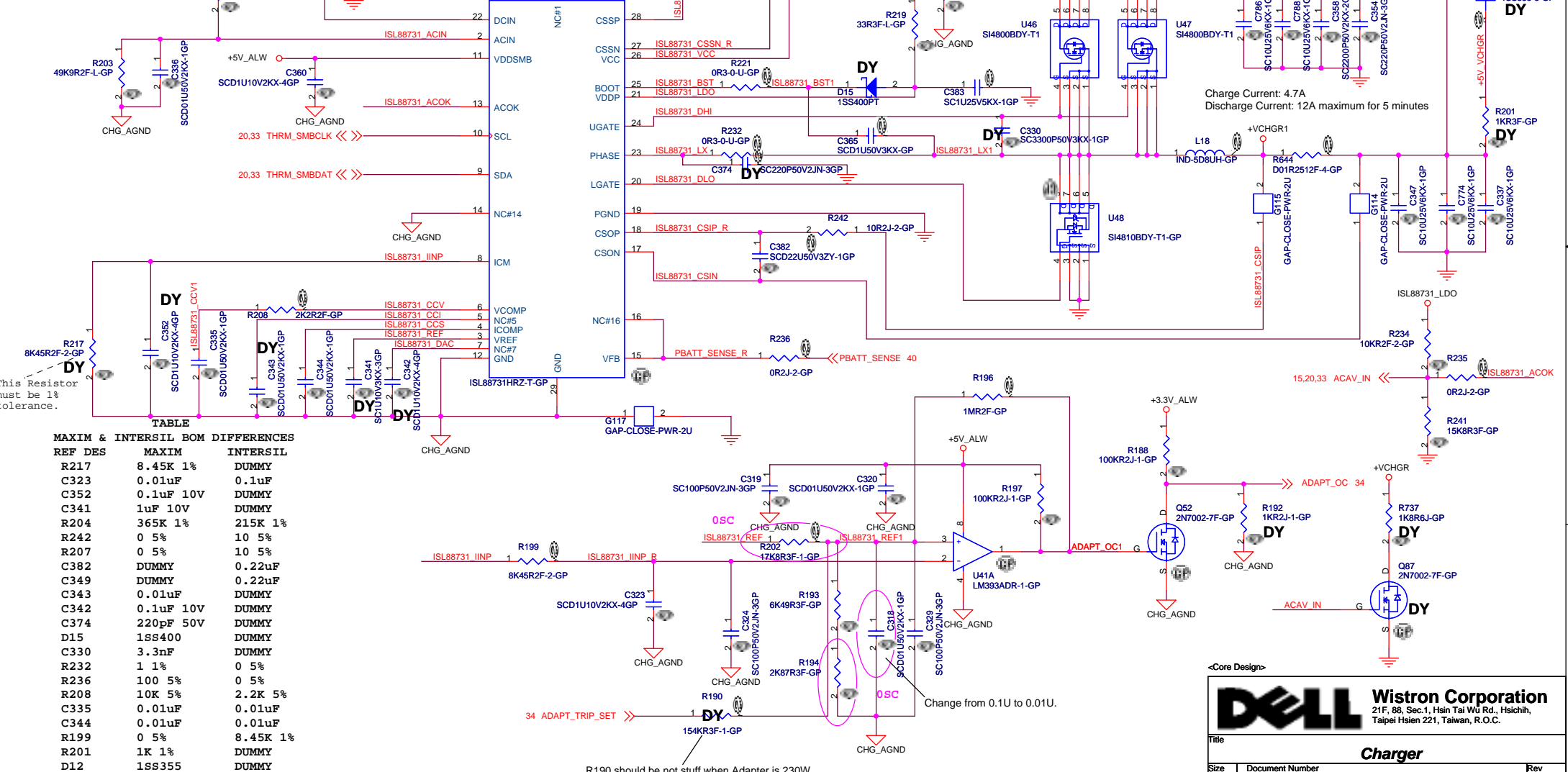
Size A3 Document Number Siberia Rev SC

Date: Friday, May 25, 2007 Sheet 40 of 50

\*PIN NAME DIFFERENCES

PIN	MAXIM	INTERMIL
1	GND	NC
3	REF	VREF
4	CCS	ICOMP
5	CCI	NC
6	CCV	VCOMP
7	DAC	NC
8	IINP	ICM
11	VDD	VDDSMB
14	BATSEL	NC
15	FBSA	VFB
16	FBSB	NC
17	CSIN	CSON
18	CSIP	CSOP
20	DLO	LGATE
21	LDO	VDDP
23	LX	PHASE
24	DHI	UGATE
25	BST	BOOT

"NC" means no-connect



TABLE

REF DES	MAXIM	INTERMIL
R217	8.45K 1%	DUMMY
C323	0.01uF	0.1uF
C352	0.1uF 10V	DUMMY
C341	1uF 10V	DUMMY
R204	365K 1%	215K 1%
R242	0 5%	10 5%
R207	0 5%	10 5%
C382	DUMMY	0.22uF
C349	DUMMY	0.22uF
C343	0.01uF	DUMMY
C342	0.1uF 10V	DUMMY
C374	220pF 50V	DUMMY
D15	1SS400	DUMMY
C330	3.3nF	DUMMY
R232	1 1%	0 5%
R236	100 5%	0 5%
R208	10K 5%	2.2K 5%
C335	0.01uF	0.01uF
C344	0.01uF	0.01uF
R199	0 5%	8.45K 1%
R201	1K 1%	DUMMY
D12	1SS355	DUMMY

<Core Design>

**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin,  
Taipei Hsien 221, Taiwan, R.O.C.

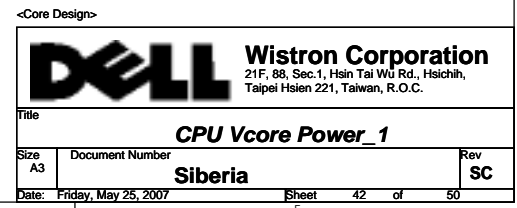
Title \_\_\_\_\_

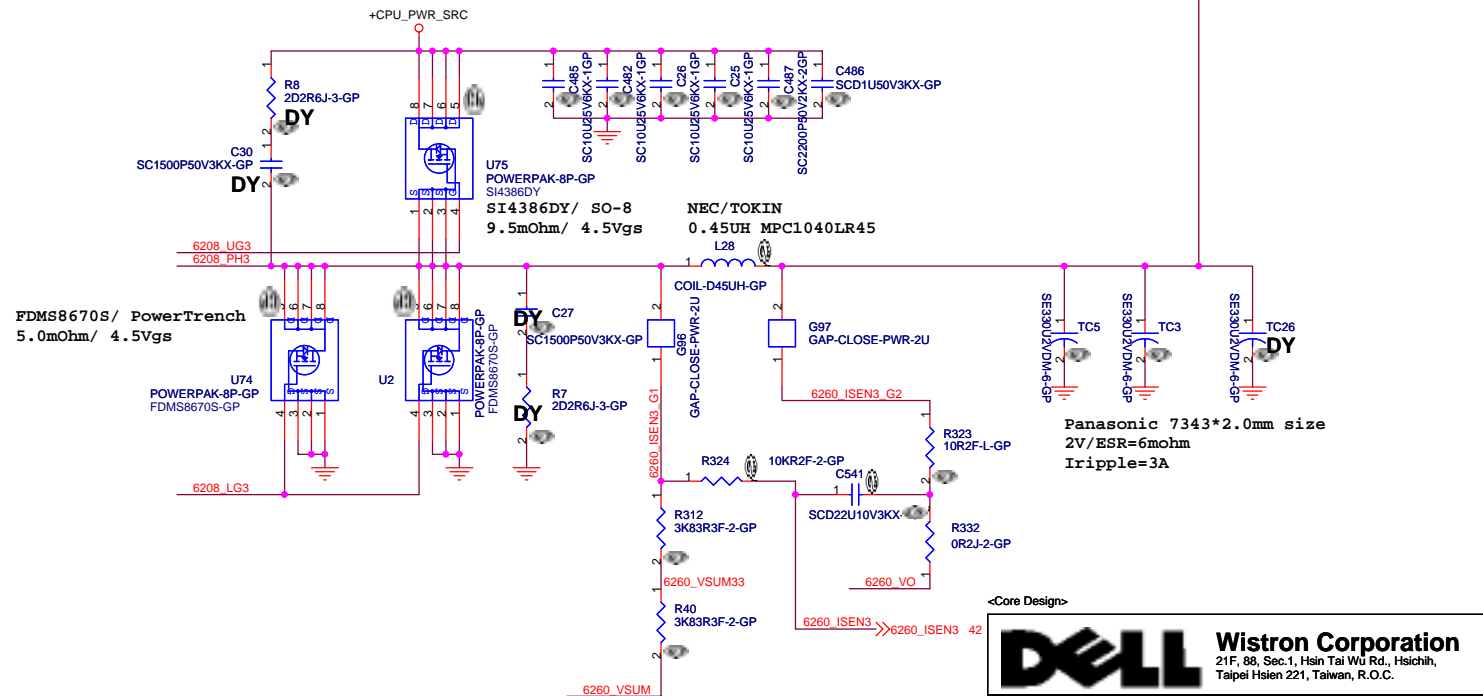
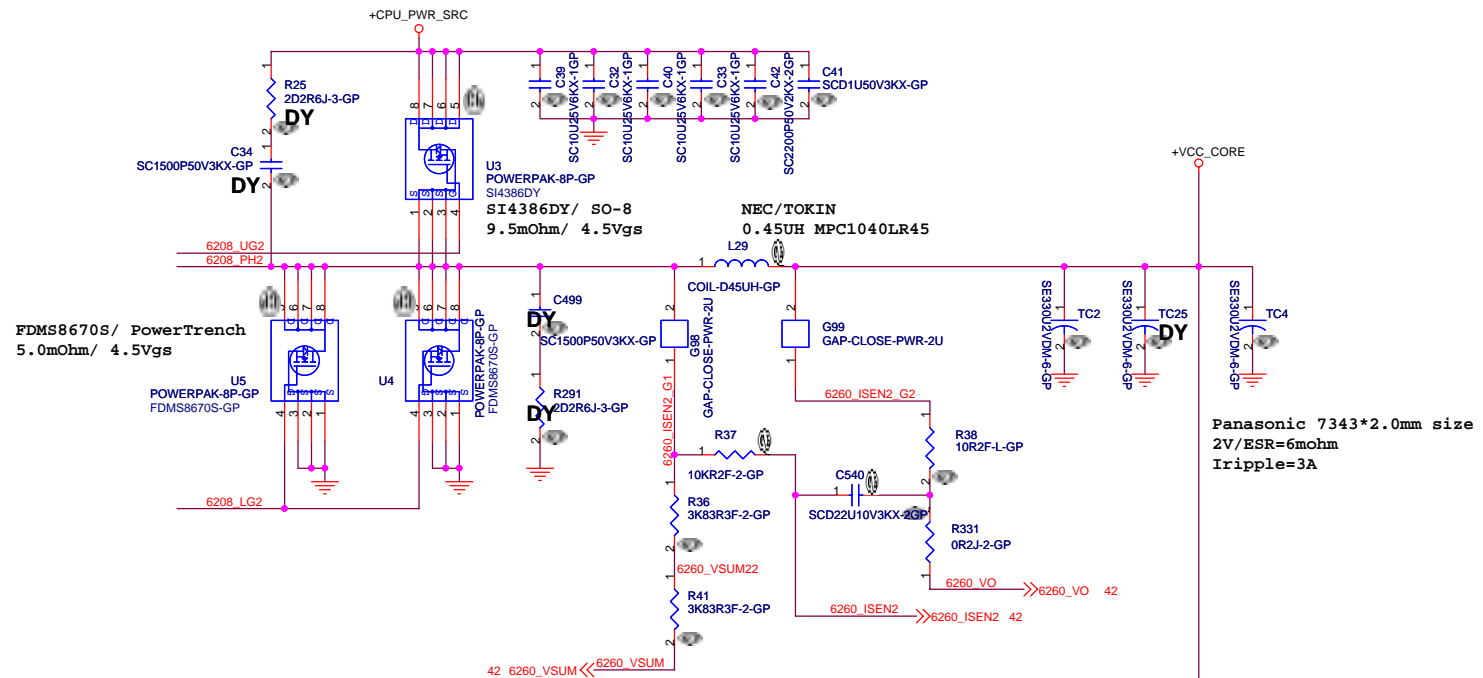
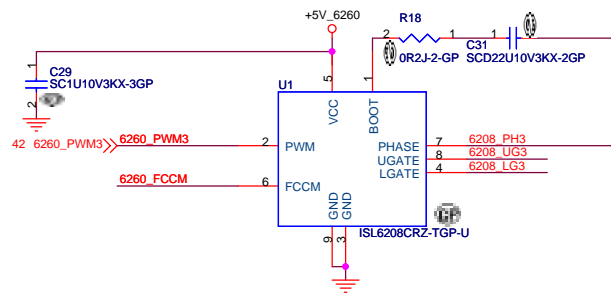
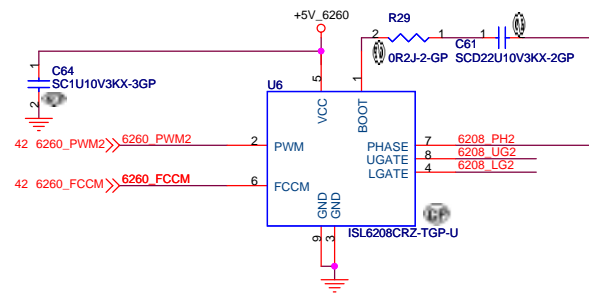
Size A3 Document Number \_\_\_\_\_ Rev SC

Date: Friday, May 25, 2007 Sheet 41 of 50

**Charger**

Siberia





<Core Design>

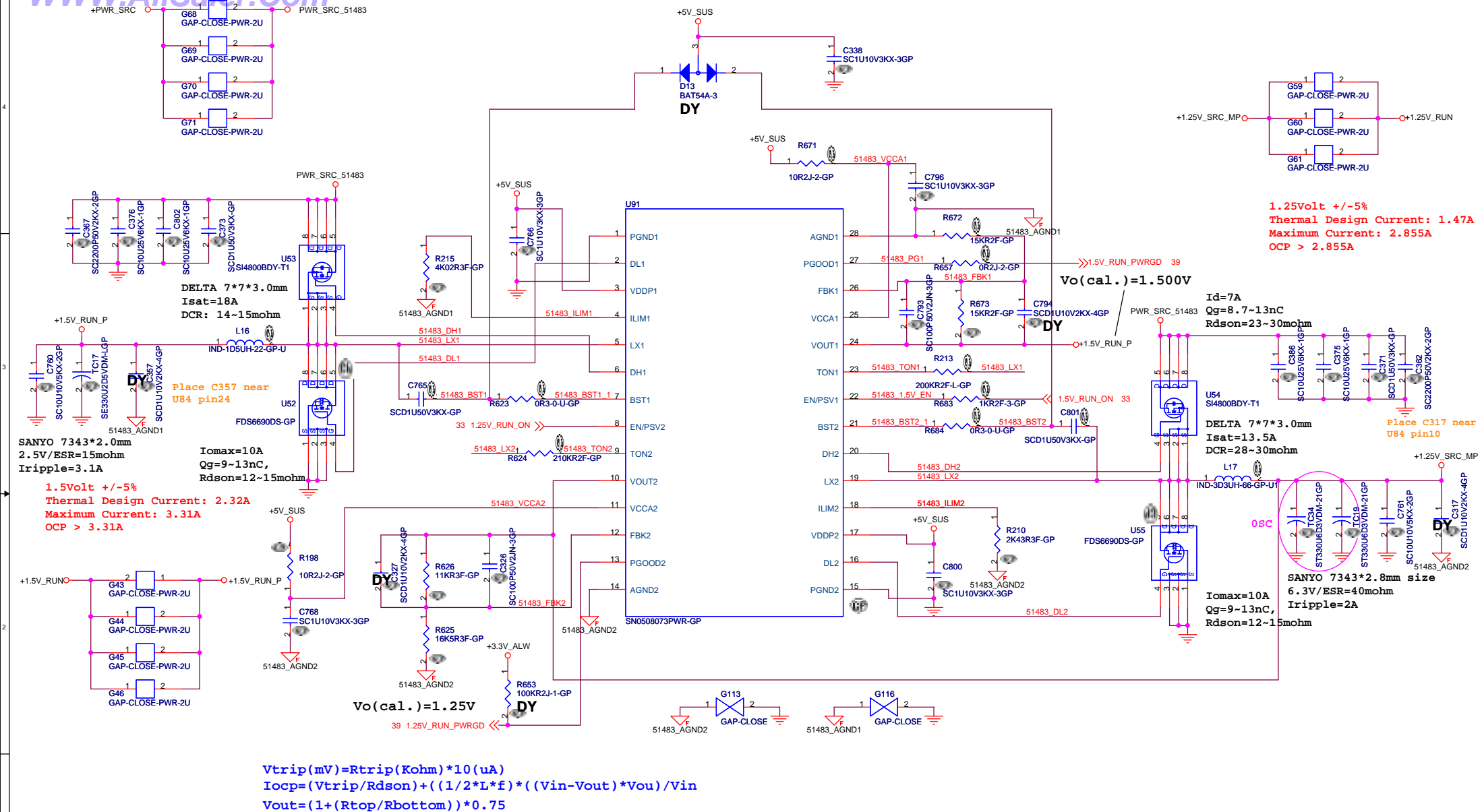
**DELL** Wistron Corporation

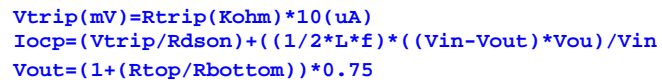
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU Vcore Power\_2

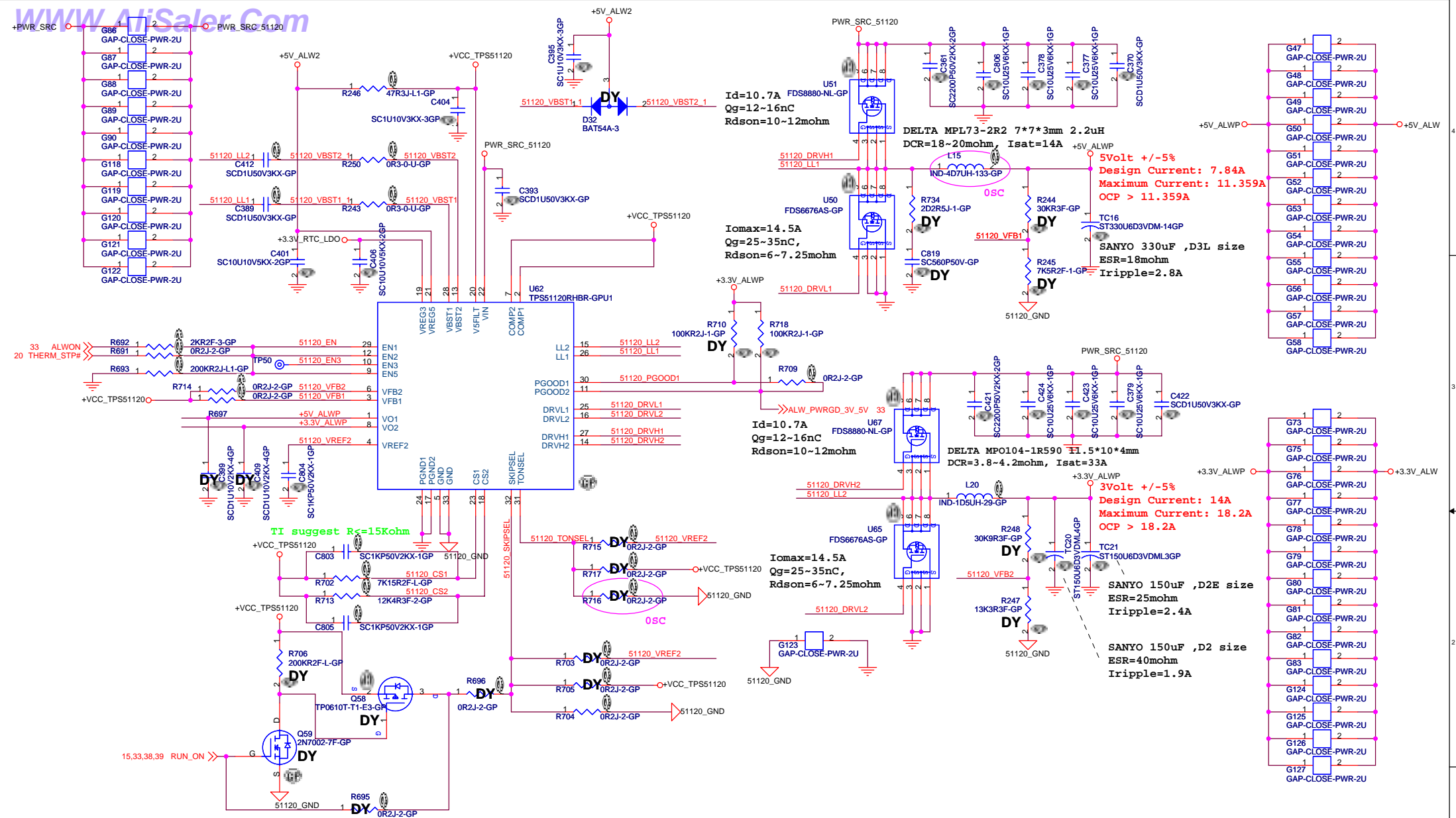
Size: A3, Document Number: Siberia, Rev: SC

Date: Friday, May 25, 2007, Sheet: 43 of 50









	GND	VREF2	PLCKT	V5FILT
SKIPSEL	AUTOSKIP	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	D-Cap MODE
TONSEL	380k/CH1 580k/CH2	280k/CH1 430k/CH2	220k/CH1 330k/CH2	180k/CH1 2870k/CH2
VFB1	N/A	not use	ADJ.	5V Fixed Output
VFB2	N/A	not use	ADJ.	3.3V Fixed Output
EN1,EN2	Switcher OFF	not use	Switchchr ON	Switcher ON
EN3,EN5	LDO OFF	not use	LDO ON	VREG3 ON

$$V_{out} = 1V * (R1 + R2) / R2$$

&lt;Core Design&gt;



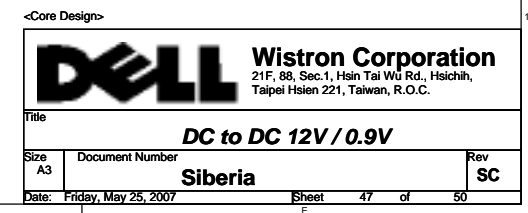
Title \_\_\_\_\_

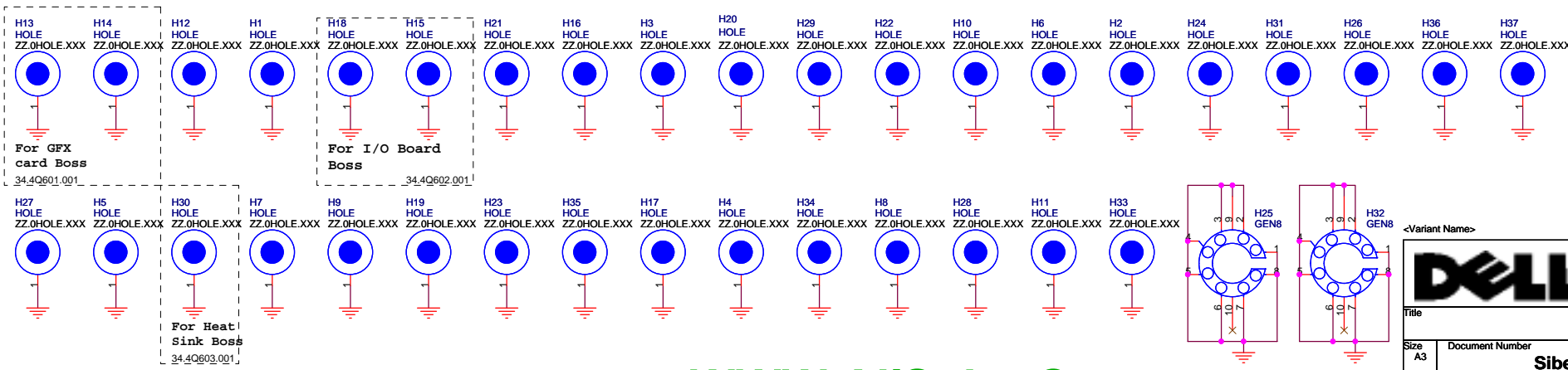
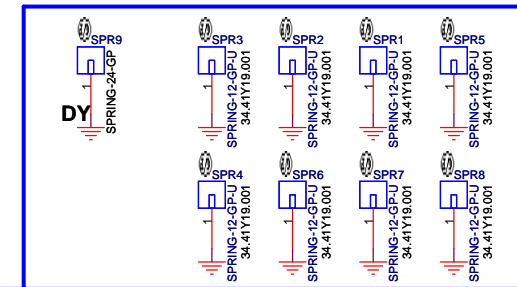
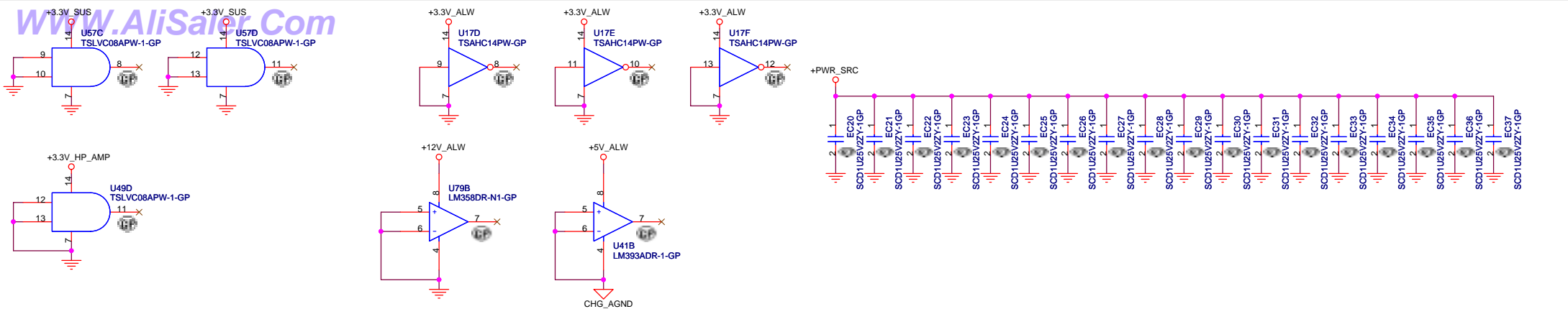
**DC to DC 3.3V / 5V**

Size A3	Document Number	Rev
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AS	<b>Siberia</b>	SC
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Date: Friday, May 25, 2007 Sheet 46 of 50





<Variant Name>

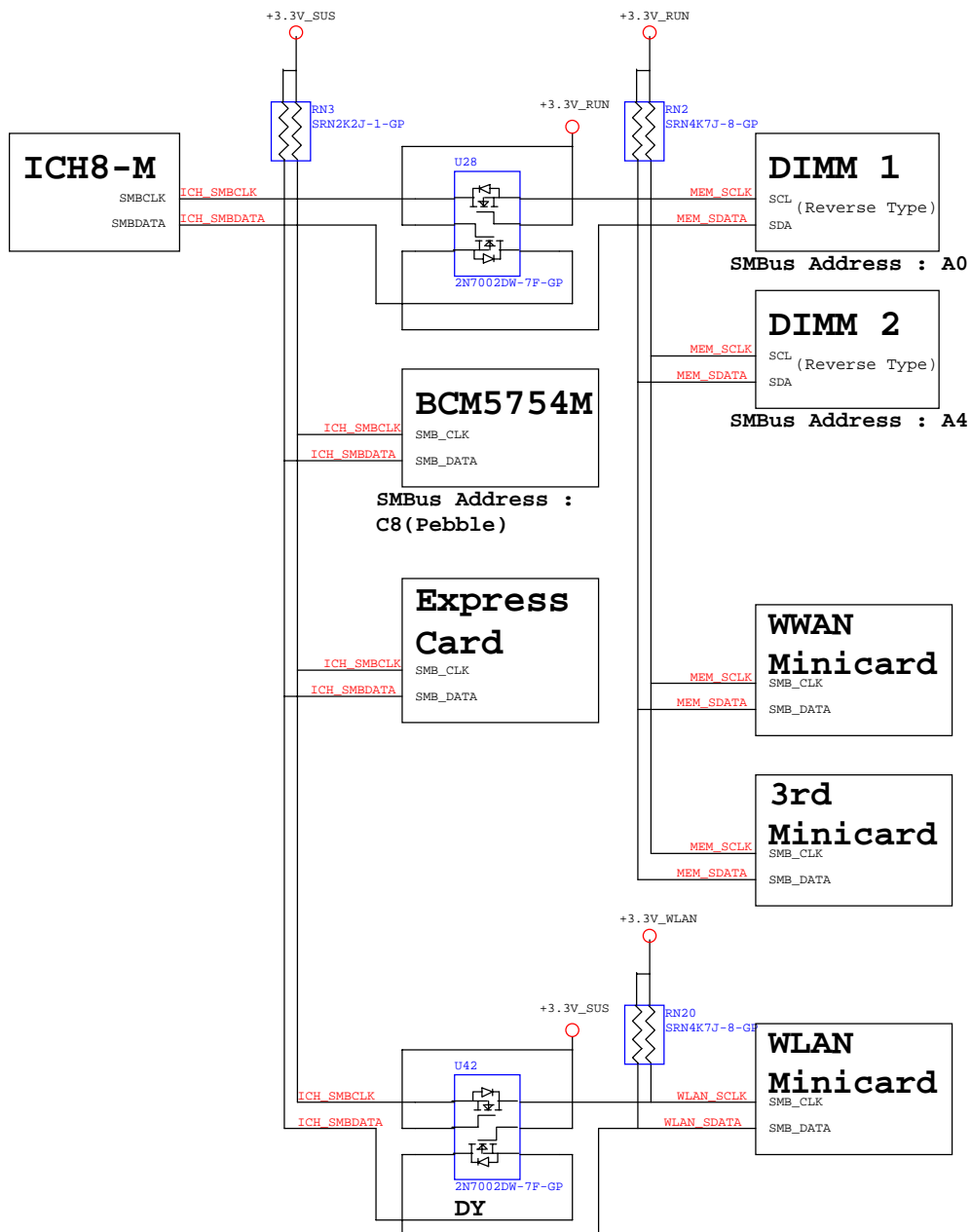
**DELL** Wistron Corporation  
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: \_\_\_\_\_

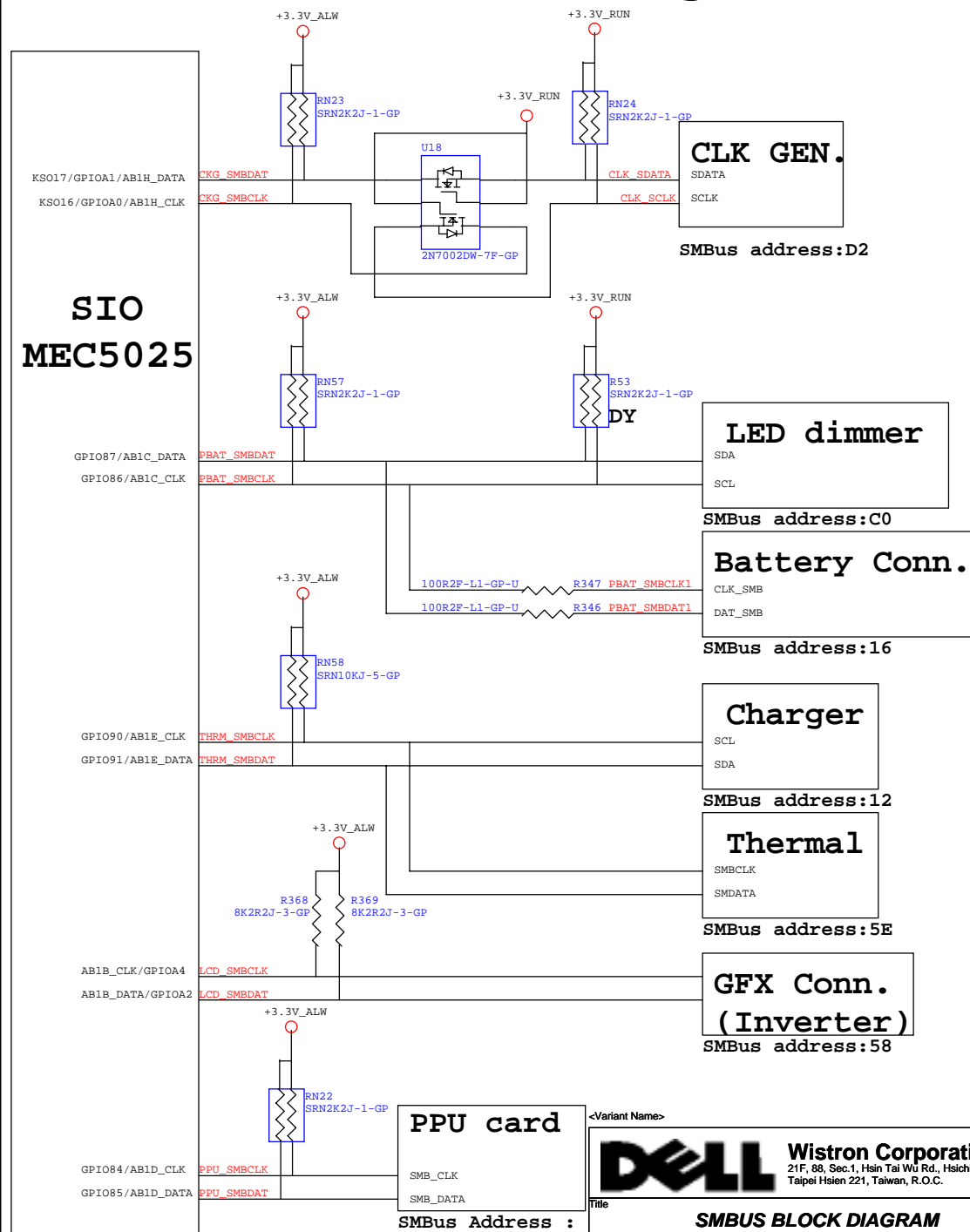
Size: A3 Document Number: **Siberia** Rev: SC

Date: Friday, May 25, 2007 Sheet: 48 of 50

# ICH8 SMBus Block Diagram




# KBC SMBus Block Diagram



DATE	VERSION	ITEM	PAGE	Modify List	Issue Description	OWNER
2007/05/15	X01 to X02	1	41	Change C318 to 0.01U and change R202 to 17.8K and change R194 to 2.87K.	By power team suggestion.	Power
		2	44,45	Change TC14, TC15, TC19, TC34 to 330U.	By power team suggestion.	Power
		3	47	Change C410 to 1000P 100V 0603 size.	Change to 100V because derating is fail.	Power
		4	6,10,19	Add TP123-TP134.	For NCTF.	EE
		5	31	Change ESD1.	Vendor from Semtech to Philips inside DELL PSL.	EE
2007/05/21		6	15	Add 10K ohm resistor to GND at U81 pin1.	Dell's command for SPDIF.	EE
		7	25	Populate R712 and R708, non-populate R711 and R707.	Dell's command for AUDIO noise.	EE
		8	45	Change TC8 to 77.23371.13L.	By power team suggestion.	Power
		9	46	Change L15 to 68.4R71B.10K.	By power team suggestion.	Power
2007/05/22		10	45	Change R560 from 150K ohm to 226K ohm.	Slow down +1.05V_RUN frequency from 600KHz to 400KHz.	Power
		11	46	Non-populate R716.	Slow down +3.3V_ALW frequency from 580KHz to 330KHz, +5V_ALW frequency from 380KHz to 220KHz	Power
2007/05/23		12	25	Change C400, C413 from 0.033U to 0.047U 1206size.	Increase value of capacitor to promote audio performance.	EE
		13	27	Change R274 from 39K ohm to 0 ohm.	Change LOM supper IDDQ setting.	EE
		14	34	Non-populate R407 and R387, populate R388 and R406.	Change board ID from X01 to X02.	EE

<Core Design>



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Title

HISTORY from X00 to X01

Size  
A3

Document Number

Rev

Siberia

SC

Date: Friday, May 25, 2007

Sheet 50 of 50